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'Electronic parts of assessed quality': an outline of the BS9000 scheme

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The BS9000 scheme is the implementation of the Burghard Report and has been the subject of much consideration for many years; it is a complex scheme of specifications and approval procedures for the procurement of electronic components by military and industrial users. This article describes the scheme with emphasis on those parts that particularly concern users of electronic components. Those parts of the scheme that affect a component manufacturing organisation as distinct from a marketing operation are only briefly discussed.

Discussions are under way toward the formation of a European scheme and this may lead to changes in the U.K. scheme.

INTRODUCTION

A committee set up in 1963 by the Permanent Secretary of the Ministry of Aviation, under the chairmanship of Rear Admiral G. F. Burghard CB DSO, was satisfied that substantial benefit would result from a scheme of common standards for electronic parts for military and industrial use.

The report of the committee recommended a major change in established procedures for the specification, inspection, and approval of electronic parts for military and industrial use. The recommendations were accepted by the Government and the electronics industry in early 1966; the industry acceptance was conditional on the extension of the principles to a European system.

Manufacturers of electronic parts are represented in Europe by CEPEC* (passive components) and CEMAC** (active devices). These two organisations are working out details of a European system on similar lines to that recommended in the Burghard Report† in the U.K. The U.K. Government (Ministry of Technology) also strongly supports a European scheme of electronic parts; and France, West Germany, and the U.K. form a Tripartite Committee, a working group of which is also working towards a European scheme based on the work now in hand by CEPEC and CEMAC.

This article is concerned solely with the implementation of the Burghard Report in the U.K., in the form of BS9000.

SUMMARY OF THE BURGHARD RECOMMENDATIONS

1) That the British Standards Institution be charged with the responsibility of preparing and progressing common standards for electronic parts for military and industrial use.
2) That BSI technical committees should prepare a specification structure for electronic parts and these should conform to IEC recommendations.
3) That detail specifications for individual electronic parts should include acceptance tests for characteristics and reliability (physical, mechanical, environmental, and life tests) on a sampling basis. The more important tests would be accumulated over six-monthly periods and made available by the manufacturers of the parts in certified test records.
4) That the scheme should include a procedure for the approval of manufacturers.
5) That qualification approval is required for electronic parts supplied under the scheme.
6) That an independent inspection authority should be set up.
7) That the independent inspection authority should be responsible for the approval of manufacturers, for qualification approval and, by a scheme of delegated inspection, for assuring that the products supplied meet the specification.
8) That release notes should accompany all deliveries.

Each of the above recommendations is considered in more detail in this article.

IMPLEMENTATION OF THE BURGHARD REPORT

In April 1966, BSI was formally requested to assume the duties and responsibilities envisaged in the Burghard Report. This involves BSI in general management of the scheme, establishment and control of the inspection and approval arrangements, and the preparation of the specifications required. The specifications are being prepared by the various existing technical committees responsible to Telecommunications Industry Standards Committee (TLE/–), but to assist with the other functions, BSI has established a new committee (OC33) together with two subordinate committees (OC33/1 and OC33/2) on which industry, users and government departments are represented:

> Management Committee OC33 is responsible for supervising the implementation of the scheme and for dealing with matters of overall policy.
>
> Inspection Committee OC33/1 is responsible for organising and overseeing the inspection and approval arrangements established under the scheme.
>
> Co-ordinating Committee OC33/2 is responsible for drafting the basic specifications applicable to all electronic parts and for ensuring that all subsequent specifications prepared under the scheme are correctly formulated.

More recently a new committee has been formed as follows:

> Electronic Parts Advisory Committee (EPAC) to check that draft specifications prepared by technical committees of BSI comply with the requirements of the OC33 group of committees. The chairmen of OC33/1 and OC33/2 are ex-officio members of EPAC. The other EPAC members are *ad hoc* nominees from OC33/1 and OC33/2 together with the Chairman and Secretary of the BSI technical committee that prepared the draft specifications.

Specification structure

The specification structure recommended in the Burghard Report and being implemented by BSI consists of:

Basic or General specifications ('Block 1')
Generic specifications ('Block 2')
Detail specifications ('Blocks 3 and 4')

This structure is illustrated in Fig. 1 on page 52.

Basic or General Specifications

BSI committee OC33/2 has prepared and published:

BS9000: 1967. *General Requirements for Electronic Parts of Assessed Quality*.*

This specification comprises a general explanation of the scheme. The procedures to be adopted by manufacturers within the scheme, and common requirements covering inspection, quality control, testing, and certified test records are described.

BS9000 was reprinted in May 1969 incorporating four amendments agreed since the earlier publication.

BS9001: 1967. *Sampling Procedures and Tables for Inspection by Attributes.*

This is a copy of DEF131A and is also identical to Mil-Std-105D. The specification covers the general rules necessary for the production sampling by attributes of electronic parts of assessed quality.

PD6435: *Instructions to Technical Committees for the preparation of Generic Specifications for Electronic Parts of Assessed Quality.*

This document gives guidance to BSI Technical Committees on the preparation of generic specifications to ensure, as far as possible, uniformity in content.

OC33/1 has prepared and published:

BS9002: 1969. *Qualified Parts List for Electronic Parts of Assessed Quality* (*including List of Approved Firms*). This document was published in July 1969 immediately after the publication of the first generic specification (BS9070: 1969 for Capacitors) and contains the list of Manufacturers, Test Houses and Stockists approved for the family of capacitors included in BS9070. (For further descriptions of generic specifications, see next section.)

Additions to BS9002 will be published regularly and BSI has arranged a subscription scheme so that all interested parties can obtain the amendments as published.

The Qualified Parts List is presented in a manner which will ensure rapid identification of specific electronic parts for particular applications.

PD6349. *Manual of Administrative Procedure for Implementation of BS9000.*
Part 1 of this document, '*Manufacturing Organisation*' gives guidance to manufacturers wishing to supply electronic parts to BS9000 specifications.

Finally OC33 has sponsored, and BSI has published:

PD6436: '*A Guide to the BS9000 Scheme*'.

This document has no legal status in the BS9000 specification scheme but gives a guide to the whole scheme. Mention is also made in the guide of international aspects.

Generic specifications

Generic specifications give the general requirements for a family of electronic parts, such as capacitors, switches, resistors, valves, semiconductor devices. The term electronic part was thought to be more descriptive than electronic component but the term is not widely used and a later revision of BS9000 will probably refer to electronic components.

The generic specifications include, for a particular family of electronic parts, general matters such as terminology, letter symbols, marking of parts, eligibility for qualification approval, test methods (electrical, mechanical, environmental, endurance, etc.) and requirements or rules for drafting detail specifications.

These rules form part of the generic specifications, although they may be published separately by BSI as is the case for semiconductor devices. They contain the minimum mandatory requirements for detail specifications

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*Committee of European Associations of Manufacturers of Passive Electronic Components.
**Committee of European Associations of Manufacturers of Active Electronic Components.
†'Second report of the Committee on Common Standards for Electronic Parts' S.O. Code No. 47–267.

*'Electronic Parts of Assessed Quality' is the official term for the scheme; the term 'Burghard System' is deprecated.

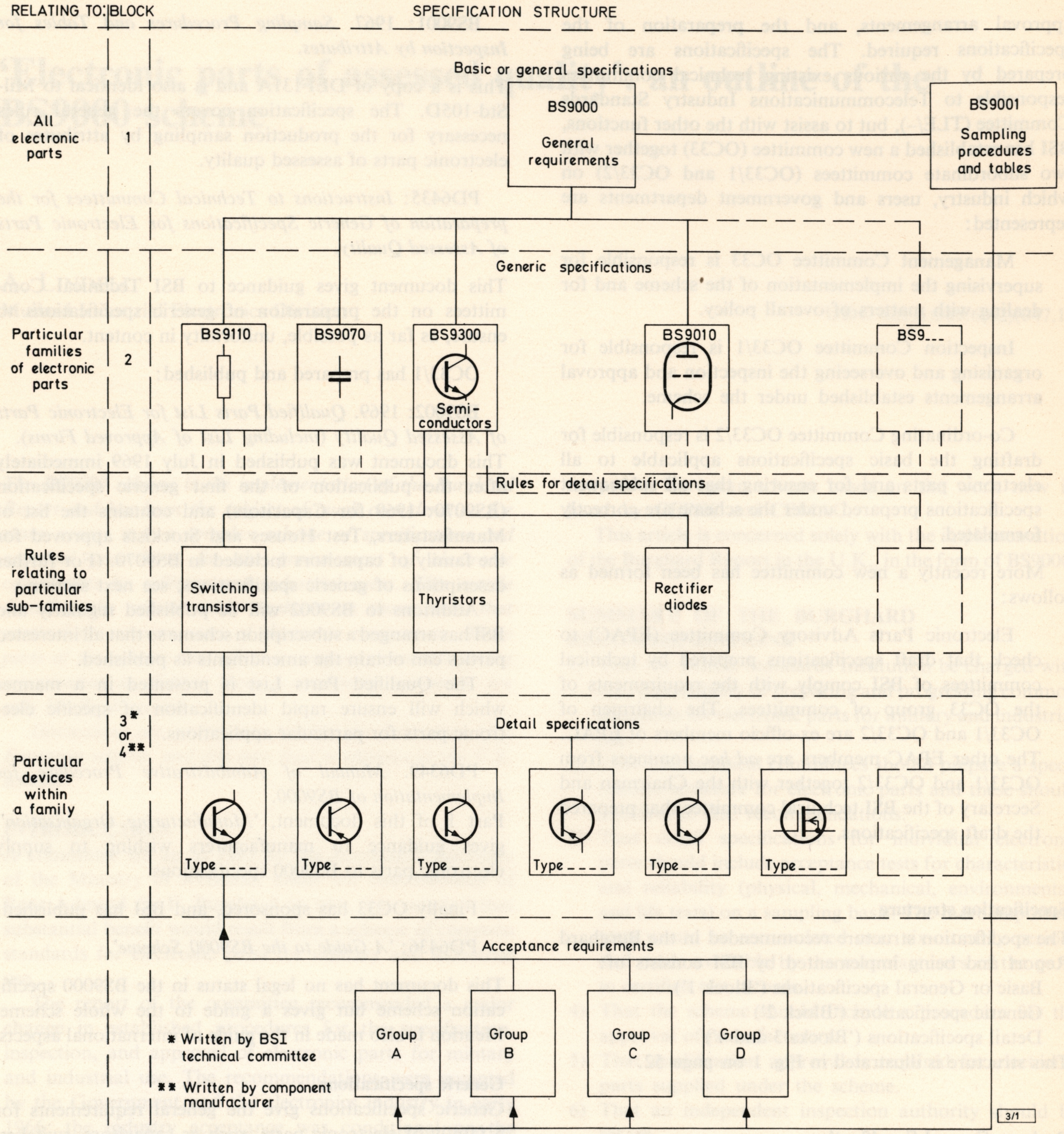

Fig. 1—Specification structure

for electronic parts or for a range of electronic parts of one family, and must be followed in the preparation of detail specifications.

The preparation of generic specifications and their associated rules documents is the responsibility of the individual BSI electronic technical committees (TLE). For example, TLE/4 is responsible for resistors and capacitors, TLE/5 for valves, TLE/12 for discrete semiconductor devices and TLE/17 for integrated circuits.

The Committee known as Telecommunication Industry Standards Committee (TLE/–) is responsible for the technical content of all generic specifications prepared by the TLE group of committees, and Committee OC33/2 is responsible for the coordinating of such specifications within the BS9000 system.

Four generic specifications were published in 1969. They are:

BS9070 '*Fixed Capacitors*' published in May 1969
BS9300 '*Semiconductor Devices*' published in July 1969
BS9500 '*Sockets for Plug-in Devices*' published in September 1969
BS9110 '*Fixed Resistors*' published in November 1969

Some Rules Documents were also published in 1969, including some for subfamilies of semiconductor devices in the BS9301 series.

Detail Specifications

A detail specification is derived from a generic specification and covers a particular part or a particular range of parts. It describes the part or parts, and gives ratings, characteristics, and the acceptance test requirements in accordance with the rules associated with the generic specification.

Application Categories

It would be impracticable to cater for the circuit and environmental test requirements for all military and industrial users in one common specification. The Burghard Report therefore envisaged three application categories, and these have been implemented in BS9000 as follows.

General Application

Parts in this category are intended to have electrical, mechanical, environmental, and endurance (life test) performance adequate to meet the needs of 60% of military and 80% of industrial applications.

Special Application

Parts in this category are intended to have a performance meeting the needs of the more sophisticated user—military or industrial; for example, for missile or space applications.

The specification for this category will normally be obtained by adding supplementary tests to the general application category and/or requiring greater stress or better assurance.

Commercial Application

Parts in this category are intended for use where lower stress levels will be met or where a lower assurance than is given by the general application category is appropriate.

This application category is not intended for the consumer or entertainment type of application, since parts for these applications are likely to be offered outside the BS9000 system. The Post Office has in the past expressed interest in this commercial application category.

Layout and content of detail specifications

Detail specifications will be prepared and printed with a common layout on A4 paper. The acceptance requirements are divided into four groups of tests:

Group A Tests

The tests in this group are on a lot-by-lot basis and include the more important characteristics (usually electrical).

Group B Tests

The tests in this group will also be on a lot-by-lot basis and will include inspection requirements for mechanical interchangeability of the part and its ability to withstand such environmental stresses and endurance tests as can be completed in one week.

Group C Tests

The tests in this group cover the inspection requirements for those electrical, mechanical, environmental, and endurance tests appropriate for inspection at intervals of three months.

Group D Tests

These tests are similar to Group C tests, but are appropriate for inspection at intervals of one, two, or three years.

Publication of Detail Specifications

Detail specifications may be prepared in two ways:

By a BSI technical committee

Detail specifications for parts made by more than one manufacturer and meeting the needs of a number of users are written by a BSI TLE technical committee. These specifications have been known as Block 3 specifications.

The specifications will include, as a minimum, all the requirements in the appropriate rules section of the generic specification. They will be published by BSI and given a number of the form BS9xxxNxxx.

By a manufacturer

A detail specification for a part can be prepared by the manufacturer of the part. These specifications have been known as Block 4 specifications. The detail specifications must include, as a minimum, all the requirements in the appropriate rules section associated with the generic specification. The manufacturer's chief inspector is responsible for ensuring that the detail specification conforms to all requirements and that a notice of intention to start qualification approval tests has been given. When qualification approval has been given, a specification number of the form BS9xxxFxxx will be allocated.

The detail specification will be published by BSI and will be distinguished from a Block 3 detail specification solely by the appearance of the name of the manufacturer instead of the reference to BSI on the title page and by the letter F in the specification reference instead of the letter N.

Block 4 specifications will be made available through normal commercial channels from bulk copies supplied by BSI to manufacturers.

Rules Documents

It will be appreciated that the rules for drafting detail specifications, associated with the generic specifications, completely control the detail specifications. There has been much consideration in BSI of the minimum test requirements to be included in these rules. In a perfect scheme, the requirements for a general application (the most important) would be similar for all kinds of component (resistors, capacitors, semiconductor devices, switches, etc.) that would be used together in a particular piece of equipment. For example, some essential electrical characteristics would be needed in Group A of the detail specification; in Group B one may expect to see tests to give some assurance about dimensions for mechanical interchangeability, about solderability, about strength of lead terminations, about mechanical robustness (vibration fatigue or shock or bump), about endurance (life) tests, and so on; Group C may contain clauses to give some assurance on the less important electrical characteristics or those that are expensive to test, on longer term endurance tests, and so on; Group D may contain those tests that control the design of the electronic part (for example, fire risks and long-term endurance).

We do not live in an ideal world, and the BS9000 scheme is not and will not be perfect. At the moment, the requirements as stated in the rules being discussed for different electronic parts for the general applications category differ widely, and the position is further complicated by the generic specification for discrete semiconductor devices (BS9300) which divides the general application category into two parts known as 'P' and 'Q'. It would be wrong to imply that this means four application categories for semiconductor devices. In fact the commercial application category is unlikely to be used and the general application category (that is both 'P' and 'Q') will cater for over 95% of all military and industrial applications. However, this makes the comparison of technical requirements for different families of electronic parts even more difficult.

A further explanation of the 'P' and 'Q' categories for semiconductor devices may be appropriate.

The 'P' category is intended to cater for most military applications (similar to CV specifications) and compared with 'Q' requires a better assurance (inspection level I, AQL 0·65% compared with S4, 1·5%) for the 160 hours lot-by-lot endurance (life) test together with additional lot-by-lot environmental tests and electrical characteristics.

The 'Q' category will cater for industrial applications, together with Post Office requirements, and a number of military applications.

The 'P' specification thus corresponds roughly to CV specifications and the 'Q' version to batch released industrial devices.

The 'P' and 'Q' versions will have different specification reference numbers (that is in the serial numbers following the letter 'N' or 'F') and only practical experience will demonstrate the wisdom or otherwise of this subdivision. If it proves valuable it will probably be extended to other families of electronic parts; if it does not prove valuable, then it will be changed.

Certified Test Records

Included in the terms of reference for the Burghard Committee was the consideration of the reliability of electronic parts.

To assure a failure rate of 0·1%/1000 hours at 90% confidence requires nearly 4000 parts to be tested for 1000 hours with no more than one failure. Many applications need an assurance of failure rate much better than 0·1%/1000 hours; to include specification requirements for such an assurance of failure rate is just not a practicable proposition for electronic parts at a price that the average user is prepared to pay.

The U.S. Mil-Std scheme gets over the problem for some electronic parts (for example resistors) by granting qualification approval to a component on the basis of an assessed failure rate (starting at 1%/1000 hours) at a confidence level of 60%, and requiring acceptance tests to maintain this maximum failure rate at a confidence level of 10%. Assurance of lower failure rates in 10-to-1 steps is obtained by accumulating component hours, assuming that the failure rate is independent of duration.

The Burghard Committee considered this method, and recommended instead a scheme of certified test records (CTR). The CTRs will contain the more important test results that the manufacturer obtains when testing his components to the detail specification. These results are accumulated over a six-month period and are presented as: number of electronics parts tested and number of failures. The cumulative results are also added for periods up to three years.

CTRs are mandatory in the BS9000 system for parts supplied to the general and special application categories and must, as a minimum, include the test results for the longer-term endurance tests (1000 hours and over). Test results obtained from other tests—for example, solderability, strength of terminations, vibration—may also be required in terms of number tested and number failed.

The CTR will also contain information about spreads of characteristics, and these will usually be presented in the form of a group frequency table. This information is mandatory for the more important characteristics before and after the longer-term endurance tests, but additional spread information on other characteristics may also be required.

The requirements for information in the CTRs are recorded in the rules documents and hence in the detail specifications. The CTRs will be published and made available by the manufacturer.

Manufacturers of equipment will thus have some information available, on an historical basis, of the quality and reliability of a particular manufacturer's product, and thus an additional factor that can be taken into account when ordering electronic parts. Government departments have said that they would expect to take account of the technical assessment of the CTR in selecting manufacturers to be invited to tender or in awarding contracts. The 'call-off' from Government running contracts might be jeopardised if the CTR indicated a significant deterioration in quality and reliability.

Independent Inspection Authority

The Burghard Committee envisaged an inspection authority independent of electronic part manufacturers and of the users of such parts. This authority would ensure that the same standards of discipline were used among all those participating in the scheme.

BSI committee OC33/1 is the inspection authority, and it has appointed as its agent to implement the requirements of BS9000, the Electrical Quality Assurance Directorate (EQD) of the Ministry of Technology. EQD has a nationwide organisation of inspectors and is an obvious choice for the scheme. EQD has, of course, responsibilities outside the BS9000 scheme, but within the BS9000 scheme it is answerable to BSI committee OC33/1.

The inspection authority will be concerned with the approval of manufacturers, with qualification approval of electronic parts, with routine acceptance tests, and with the authentication of certified test records.

In the BS9000 system, EQD plays the same role as that of an auditor in the financial world.

Approval of Manufacturers, Test Houses, and Stockists

An electronic part manufacturer wishing to take part in the BS9000 scheme must meet certain general requirements in respect of inspection staff, test equipment and facilities, quarantine and bonded stores, inspection records, and so on, and these are described by the manufacturer in a quality assurance manual.

The manufacturer's chief inspector must meet minimum standards of competence and integrity and be responsible for a well-ordered inspection department. The chief inspector is the principal link between the manufacturer and the BSI, and it is his sole decision whether a particular part may be released for delivery. The chief inspector is responsible for ensuring that released products meet the specification, that a manufacturer's specification conforms to the requirements of the generic specification, and that the CTRs are accurate.

Manufacturers will be approved for the supply of a particular family of electronic parts as described in a generic specification, and will be expected to have test equipment described in the specification and adequate means of calibration. Where a manufacturer lacks facilities for certain tests, arrangements can be made for these to be carried out by an approved test house. The approval of a test house follows a similar pattern to that of a manufacturer.

A number of stockists may wish to supply electronic parts meeting the BS9000 requirements. Approval of such stockists follows a similar pattern.

Arrangements have been made for manufacturers, test houses, and stockists to apply for approval under the BS9000 system when a draft generic specification is issued for comment by BSI.

By May 1969 when the first generic specification was published, there had been 165 applications for approval; 119 from manufacturers (mainly of resistors, capacitors and semiconductor devices); 10 from test houses and 36 from stockists. With the publication of the generic specifications some of the applicants have been formally approved and their names appear in BS9002 or in the monthly amendments to BS9002.

Qualification Approval of Electronic Parts

Qualification approval is the status given to a design of electronic part (or range of parts) which has been shown to meet all the requirements of the relevant specifications. Electronic parts supplied against the BS9000 scheme must first have qualification approval.

To obtain qualification approval an approved manufacturer demonstrates, in a qualification approval test report, that he can meet the detail specification for all Group A, B, C, and D tests that can be accomplished in 1000 hours. Electronic parts with qualification approval will not therefore be available until about three months after the publication by BSI of the relevant generic specification and, more important for the preparation of detail specifications, the associated rules document. Thus the first electronic parts available for purchase to BS9000 are unlikely before January 1970.

As electronic parts receive qualification approval they will be included in the monthly amendments to BS9002.

Eligibility for Qualification Approval

The whole of the BS9000 concept implies professional control of production in all its stages. Electronic parts which are imported from overseas and merely tested to a BS9000 detail specification (with the good ones being delivered) are clearly therefore not eligible for the BS9000 system. On the other hand it would be unreasonable to expect the approved manufacturer to carry out all processes himself from incoming raw materials. Somewhere between these two extremes is a stage which can be defined as that which makes an electronic part eligible for qualification approval under the BS9000 scheme.

BSI and BS specifications can only be concerned with technical matters but the subject of eligibility has commercial overtones and, more recently, political considerations have made agreement more difficult. The result of this has been that it has taken about two years to get agreement on this clause and has delayed the publication of generic specifications by up to a year.

The agreed clause (2.3.2(3) in BS9000) requires the generic specification to define a 'first stage of processing, which shall be either the assembly of piece parts or an earlier stage of processing where this is essential to the quality of the finished product. This stage and all subsequent processes shall be carried out under the direct surveillance of an approved chief inspector . . .'.

Two exceptions follow:

(i) to allow subcontracting of a subsequent process when this is identified as such in the generic specification

and

(ii) where the first stage or subsequent stage (not identified in the generic specification) is not carried out under direct surveillance of an approved chief inspector then a procedure has to be worked out with EQD to satisfy BSI (OC33/1) that the quality of the product is not impaired.

Provision is made for the generic specification to exclude this route (ii) and BSI committees are required (BS9000:1.4.2) to review at annual intervals the implementation of this route where the generic specification does not already exclude its implementation.

When route (ii) is used, details of the scheme of surveillance have to be recorded on the qualification approval certificate, copies of which may be obtained from BSI on request (BS9000:2.3.5), and the qualified parts list (BS9002) has to be annotated.

The generic specification for discrete semiconductor devices (BS9300) excludes route (ii), but refers to route (i) by identifying plating of fully encapsulated devices as a process that can be subcontracted (BS9300:1.1.7).

Discussion of this difficult subject is certain to continue. The writer believes that some alleviation of the problem could be obtained by separating electronic parts into those that are assembled items (such as switches, relays and connectors) and those that are essentially processed items (such as semiconductor devices, resistors and capacitors). Different clauses for eligibility could then apply to each type.

There has been much heart-burning about this 'U.K. made' concept. The Ministry of Technology has pushed strongly the alleged importance of making sure that the manufacturer has all the essential operations of manufacture under his control to ensure a high-quality and reliable product.

Acceptance Inspection

After the completion of a successful qualification approval exercise, an approved manufacturer may supply, against orders for BS9000 specified parts, only those parts that meet the full requirements of the relevant detail specification. To do this, he collects the manufactured electronic parts into identifiable lots, and on every lot carries out the tests specified in Groups A and B of the specification. The inspection level (IL) given for each clause of the specification determines the sample size, and the lot is acceptable for this clause if the number of rejects in the sample is not more than a particular number determined by the acceptable quality level (AQL). For example, if the IL is I and the AQL is 1·5%, and the lot size is 5000, the tables of sampling plans in BS9001 indicate that 80 specimens from the lot are taken at random. The test is carried out to the limits specified, and the lot is acceptable for this clause if not more than 3 rejects are obtained. This operation is repeated for all the clauses in Groups A and B on the lot, and the lot can only be released for delivery if the tests are satisfactory for all clauses.

Every three months, Group C tests are carried out; and at intervals of one, two, or three years (as specified), Group D tests.

Testing can be reduced if the product is good enough to meet the requirements in BS9001 for reduced inspection; and a further reduction in testing is possible for electronic parts of similar design—that is, if they are structurally similar.

Some manufacturers have operated similar disciplines for their industrial products for many years, but the chief inspector has used discretion—usually in agreement with the customer—when a particular lot does not meet all the requirements. No discretion is given to the chief inspector in the BS9000 scheme.

Release Notes: Certificates of Conformity

Direct purchases by the Government involve an elaborate paperwork system. The Ministry of Technology uses documents known as 640 forms. These consist of many pages of forms, some of which are used to ensure that the product meets the contract requirements and others for payment. The Ministry of Defence (Navy Department) uses a similar set (D55 forms). These systems are incompatible with modern mechanised paperwork systems.

The preparation of release notes for all deliveries is a requirement of the BS9000 scheme, where the term 'Certificates of Conformity' is used. The scheme employed is less incompatible with modern paperwork systems, but for direct purchases of electronic parts by the Government to BS9000, the 640 and D55 forms may still be necessary.

The certificate of conformity certifies that the parts supplied meet all the requirements of the relevant BS9000 specifications, and includes information whereby the delivered batch can be traced back to the manufacturer's test records.

Mark of Conformity

Consideration is being given by the committees OC33/1 and OC33/2 to a mark of conformity instead of a certificate. This has been prompted by the progress being made towards a European system which includes a definite preference for a mark on the electronic component (where the component is big enough), or on a sealed package containing smaller electronic components, instead of a certificate. The mark, together with other required information, allows the manufacturer's test records to be traced, in the same way as a Certificate of Conformity would.

No firm proposals have yet been made for the amendment of BS9000 to include this release procedure and an amendment is unlikely before about the middle of 1970 when possibly other amendments may reflect the revision of BS9000 to make it compatible with a European scheme.

GENERAL OBSERVATIONS ON THE BS9000 SCHEME

The Government has taken a leading part in all aspects of the BS9000 scheme. It accepted the Burghard Report in March 1966, and has dismantled its authorities for DEF, CV and CN specifications for passive components and active devices. Not unnaturally, Ministry of Technology and Ministry of Defence representatives on BSI committees have been very vocal to ensure that Government requirements are included in the BS9000 scheme.

A Government White Paper issued by H.M.S.O. in May 1967, entitled 'Public Purchasing and Industrial Efficiency' (Command 3291), opens by saying 'It is the Government's policy to help to make British industry more efficient and competitive'. Section 9 of the paper starts off by saying 'Reduction in the number of similar varieties of products purchased is a powerful method of promoting efficiency in production'. The paper contains several very favourable comments on BSI activities in this field. Sections 15 and 16 headed 'Quality Assurance Schemes' state:

15. 'Standardisation is indispensable to schemes which objectively measure product quality including performance, safety and reliability, Such schemes can be extended to provide quality control, which ensures that the whole production of a particular article conforms to minimum requirements, and so removes the need for further inspection and testing by the purchaser. Schemes of this kind enlarge the market for good products, and so tend to reduce their unit cost.'

16. 'The Kitemark Scheme operated by BSI is an example. Another is the Burghard Scheme, which is being implemented by the Ministry of Technology in cooperation with other Departments, which applies standards in the assessment of electronic components. The Government will support the improvement and greater use of such schemes, and their extension to appropriate new fields.'

The policy stated in the White Paper will apply not only to the central Government; local authorities, the nationalised industries, and other public bodies will be invited to co-operate.

Effect of BS9000 scheme on manufacturers and users

The key to the success of the whole BS9000 operation rests with the industrial users.

Users of electronic parts for military applications will ultimately have to use BS9000 specifications, but in the past the same users have had available DEF, CV and CN specified parts, and the substitution of BS9000 specifications for these specifications clearly makes little difference. The whole Burghard concept has been based on the fact that the capital goods industry requires the same quality and reliability for parts as the average military user.

It has been said that purchase of electronic parts against manufacturers' data sheets does not give the user the assurance he needs. Very few data sheets indicate what tests are carried out by the manufacturer, and if this is important, clearly BS9000 specifications will help. A number of users write their own specifications, and it is hoped that the availability of BS9000 specifications will reduce this operation. Industrial users of electronic parts are represented on the BS9000 committees by trade associations like BEAMA, EEA, SBAC, and TEMA; but the more vocal representatives would appear to represent industrial users more interested in military applications.

Representatives of the consumer industry have not taken an active part in the BS9000 deliberations. Although there is no reason why the consumer industry should not use the BS9000 specifications, it is expected that the industry will obtain its requirements outside the BS9000 scheme.

Manufacturers of electronic parts who supply products for military applications will almost certainly have to take part in the BS9000 scheme, but electronic parts will still be available and supplied against manufacturers' data sheets.

Integrated video pre-amplifier, sync, a.g.c. and noise protection system for monochrome receivers

M. C. GANDER
Mullard Central Application Laboratory

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UDC 621.397.13. [621.397.62]: 621.397.335—419.7
UDC 621.397.13 [621.397.62]: 621.396.665—419.7

The TAA700 integrated circuit has been designed to perform the a.g.c., sync pulse separation and video drive functions in a television receiver. It provides a low impedance video drive, a d.c. control potential to the line oscillator and a positive-going sync pulse to the field timebase, in addition to the a.g.c. potentials for the i.f. and r.f. amplifiers. The TAA 700 integrated circuit is encapsulated in a 16-lead 'quad-in-line' package.

This article describes the application of the TAA700 in a typical monochrome receiver and details of the peripheral circuits and performance are given, including a choice of line oscillator circuits.

INTRODUCTION

An integrated circuit is economically attractive for a domestic television receiver only if it incorporates sufficient circuit functions to replace a fairly extensive area of discrete circuitry. The degree of technical attraction depends not only upon adequate performance, but, where the signal processing circuit is concerned, upon the receiver designer being given a choice in overall design; for example, the use of either valves or semiconductor devices in the output stages. The complexity of an integrated circuit is restricted by the maximum power dissipation in a given type of envelope and the number of lead-outs. The limited voltage capability of present integrated circuits precludes integration in areas approaching the high-voltage output stages.

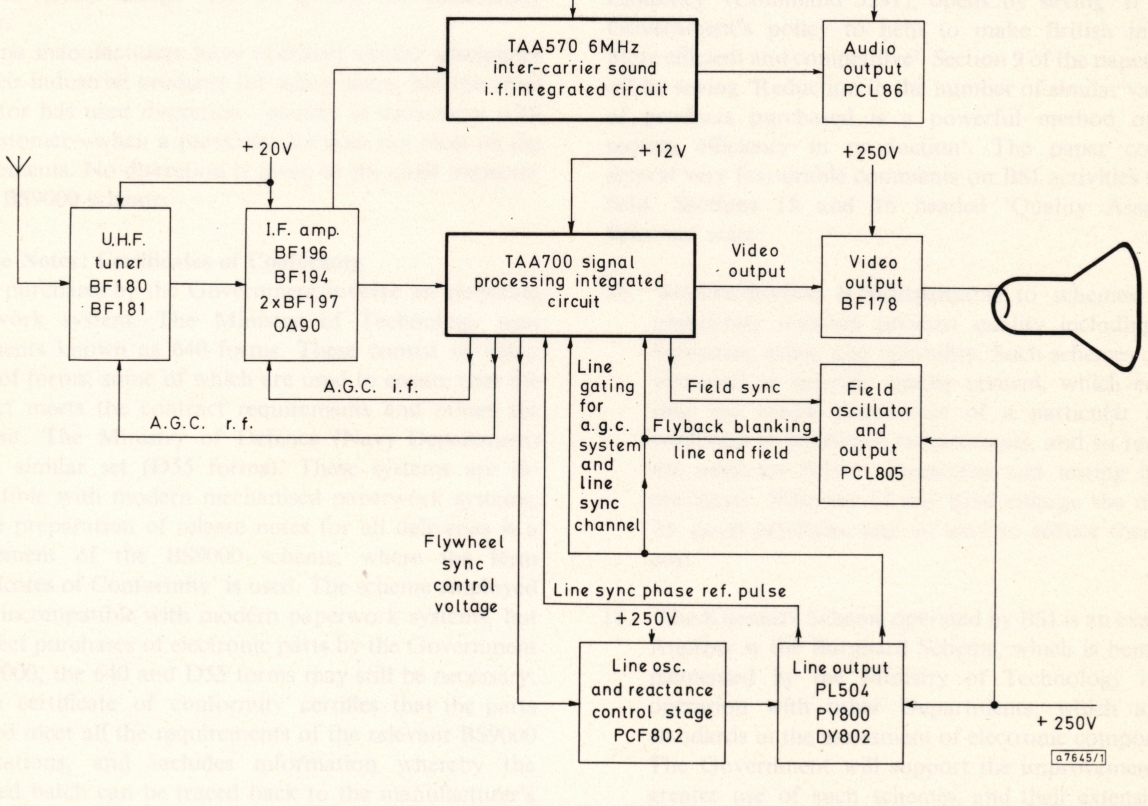

+12V
+250V
TAA570 6MHz inter-carrier sound i.f. integrated circuit
Audio output PCL86
+20V
+12V
+250V
U.H.F. tuner BF180 BF181
I.F. amp. BF196 BF194 2xBF197 OA90
TAA700 signal processing integrated circuit
Video output
Video output BF178
A.G.C. i.f.
A.G.C. r.f.
Line gating for a.g.c. system and line sync channel
Field sync
Flyback blanking line and field
Field oscillator and output PCL805
Flywheel sync control voltage
Line sync phase ref. pulse
+250V
Line osc. and reactance control stage PCF802
Line output PL504 PY800 DY802
+250V
a7645/1

Fig. 1—Block diagram of hybrid monochrome receiver

A study of monochrome and colour receivers shows that the signal processing circuit (the video pre-stages, sync pulse separator, a.g.c. system, and noise protection circuits) is characterised by low power dissipation and operation from d.c. to about 6MHz. There is no fundamental need for frequency-selective components requiring inductors in this area. The signal processing area of a receiver, therefore, lends itself to integration.

By careful choice of the circuit functions and the parameters of the output waveforms, it has been possible to design an integrated circuit suitable for receivers employing either valves or semiconductor devices in the output stages.

TAA700 CIRCUIT FUNCTIONS

The circuit functions contained in the TAA700 are as follows:

The *video pre-amplifier chain* which also provides for field and line flyback blanking.

The *a.g.c. system* is line-gated, providing a control potential for the i.f. stage, and also a delayed control potential for the r.f. stage.

The *sync pulse separator* is designed to follow fast variations of signal level.

The *noise protection system* is amplitude and frequency selective, and protects both the a.g.c. and sync channels.

The *line flywheel phase detector* comprises a symmetrical transistor which replaces the usual pair of diodes.

The *field sync pulse separator* provides a rectangular low impedance sync pulse output.

CIRCUIT DESCRIPTION

A block diagram of a typical monochrome hybrid receiver is shown in Fig. 1. Two integrated circuits are used—the TAA700 signal processing unit and the TAA570 inter-carrier sound amplifier (Ref.1). Valves are employed in the deflection and audio output circuits.

Fig. 2 shows the details of the peripheral circuits of the TAA700 for use in a monochrome receiver. In addition to the components immediately associated with the integrated circuit, details of the r.f. and i.f. gain controlled stages, the video detector, the video output stage and the line oscillator are shown because these must be matched to the TAA700.

Supply voltage requirements

The TAA700 requires a supply of +12V nominal (+14V maximum). Its nominal current requirement of 22mA can vary by plus or minus 6mA due to circuit spreads, and a.g.c. and signal conditions can cause an increase of up to 15mA from the nominal value. Allowance must also be made for the current taken by the peripheral circuits. A supply of typically 20V feeds the tuner and i.f. amplifier, and the 12V line is obtained from this by using a series dropping resistor, R_{11} (Fig. 2). The 20V supply may be obtained from a low-voltage mains transformer, by scan rectification from a winding on the line output transformer, or from the valve heater chain if it includes a series voltage dropping diode.

If the 20V supply is obtained from the valve heater chain, it is necessary to ensure that the voltage across the TAA700 is maintained within the permitted limits. During the switch-on surge the voltage across the device must not exceed 18V for the first 10 seconds and 16V for a further 20 seconds. Under normal operation the limits of +10V to +14V must be kept despite variations in a.g.c. current and mains voltage. Owing to the limited total l.t. current available (about 180mA), care must be taken to reduce the effects of mains voltage variations. These disadvantages can be avoided by using a scan-rectified l.t. supply as it has a low source resistance.

A decoupling capacitor C_3, of 125μF 16V working, is connected to pin 5 to limit any ripple on the 12V supply to 50mV.

Video signal channel

The signal from the video detector is the source of all the information required by the picture tube and deflection circuits, and is the main input to the integrated circuit. The input video signal is applied to pin 10 (Fig. 2) and is negative-going with respect to the chassis with a peak amplitude of 2V. A detector load resistor of 2·7kΩ is included in the TAA700 with an input capacitance at pin 10 of not greater than 1pF. The video detector circuit normally requires no d.c. bias voltage.

The bottom bend in the forward characteristic of a video detector diode results in non-linear operation at low signal or modulation levels, and this occurs mainly over the output range 0 to 0·75V. The video gain provided by the TAA700 permits a video input signal of about 2V peak amplitude to be used, giving adequate performance in monochrome receivers.

The detector can be operated at a higher level by using a potential divider as a diode load (connecting pin 10 to the junction of the two resistors). This reduces non-linearity to a level which is acceptable in colour receivers, or in cases where a higher sound signal level is required.

A video output signal amplitude of 6V peak-to-peak is required for driving a valve video output stage, and this is more than adequate for a video output transistor. The TAA700 provides a video output signal from pin 12 which has a peak-to-peak amplitude of 6V with its black level at +5V and black-to-white amplitude 4·2V. This output signal is produced by an emitter follower in the TAA700 and can therefore drive a video output transistor directly. To minimise the power dissipation in the TAA700 the emitter resistor is connected externally (R_{21}, value 1kΩ, in Fig. 2).

The video output stage shown employs a BF178 in a d.c.-coupled circuit. A constant black-level type of contrast control is shown, where the "cold" end of the potentiometer R_{22} is connected to a d.c. potential, derived from

R_{23} and R_{24}, corresponding to the black level of the TAA700 video output signal (+5V). The emitter of the BF178 must be biased to meet the positive sit-up of the video signal applied to its base. This is done by R_{25} and R_{26}, the parallel equivalent value of which gives the desired emitter resistance for the video transistor. A preset control R_{25b} is necessary to set the black level in the video output stage. A detailed design procedure for transistor video output stages has been described (Ref. 2).

Provision is made for flyback blanking in the TAA700 video channel. By applying positive-going line and field flyback pulses to pin 11 (greater than 1V but not exceeding 5V amplitude) via R_{19} and R_{20}, the video channel is closed during the flyback pulses so that the video output signal on pin 12 disappears. The potential which pin 12 assumes during the flyback is then determined by the potential at the junction of R_{23} and R_{24}, and the values of R_{22} and R_{21}, and is approximately +2·5V. This is sufficient to blank out the flyback lines on the picture tube under most conditions.

It has already been said that the video output of the TAA700 is sufficient to drive a valve video output stage. However, unlike the video transistor, it is uneconomical to sit up the cathode of the video valve because a high bleed current is required in the potential divider to give the necessary low value of cathode resistance. An alternative would be to earth the cathode resistor of the valve in the normal way and operate the TAA700 from a −12V line; however, it would then be necessary to operate the r.f. stages in the tuner and the gain controlled i.f. stage from the same line to secure the correct a.g.c. operation. Such an arrangement, although feasible, would complicate the receiver. A further alternative could be to replace R_{21} with the contrast control, thus retaining the simplicity of a single positive l.t. supply but necessitating a.c. coupling of the video signal to the valve.

Automatic gain control system

The a.g.c. system must control the gain of both the r.f. stage and i.f. amplifier so that the detected video signal is held at constant amplitude. For the best operation the initial control must be on the i.f. amplifier up to a predetermined attenuation, after which control must be transferred to the r.f. stage. It has been possible to incorporate the complete a.g.c. system in the TAA700, including the control changeover, and to provide two outputs to the controlled stages.

A sync-tip-level line-gated a.g.c. system has been chosen which has a threshold level (signal delay) fixed internally to maintain the detected video signal level at 2V peak amplitude. Line gating is employed to minimise the disturbance which would otherwise occur on the a.g.c. voltage during the field sync pulse group. This enables a short smoothing time-constant to be used in the a.g.c. control loop, which minimises picture disturbance during rapid signal 'flutter', and reduces the time taken for the picture to become stable after a channel change.

The TAA700 has been designed for forward control of n-p-n r.f. and i.f. transistors, that is with positive-going a.g.c. outputs. The a.g.c. control voltage outputs, from pin 4 (+8V maximum) for the BF196 i.f. gain controlled stage, and pin 6 (+7V maximum) for the BF180 r.f. stage, are connected directly to the base networks of these stages.

Before the a.g.c. system reacts to an input signal there are no outputs from pins 4 and 6; therefore the initial maximum gain conditions for the i.f. and r.f. stages are determined entirely by their d.c. bias networks: R_1, R_2, R_3, R_4 in the r.f. stage and R_6, R_7, R_8, R_9 in the i.f. stage. For the BF180 and BF196 these values have been chosen to give initial transistor emitter currents of 2·5mA and 3mA respectively.

In the TAA700 the r.f. a.g.c. voltage cannot exceed the i.f. a.g.c. voltage (P. 64). Thus these stages must be designed so that sufficient a.g.c. voltage is available to achieve the desired gain reduction (at optimum signal-to-noise ratio) in the r.f. stage when the i.f. stage is fully controlled. For adequate gain reduction in the BF180 for u.h.f. operation, an emitter current of around 12mA is required, therefore with an emitter resistor of 390Ω (R_2), some +5·5V output is required from pin 6. This can only be obtained if the i.f. a.g.c. voltage is at least +6·5V. The emitter current required in the BF196 for adequate gain reduction in the i.f. stage is about 12mA and thus, with a base potential of +6·5V or more, an emitter resistor of 470Ω (R_7) is needed. These resistor values are high enough to provide adequate d.c. stability of the non-controlled working points.

The level at which take-over from i.f. to r.f. control occurs is set by the potential from R_{14} applied to pin 7. It may be possible to replace R_{14} with a fixed potential divider after gain and attenuation tolerances in the i.f. amplifier and required signal-to-noise ratio have both been considered for a given receiver design.

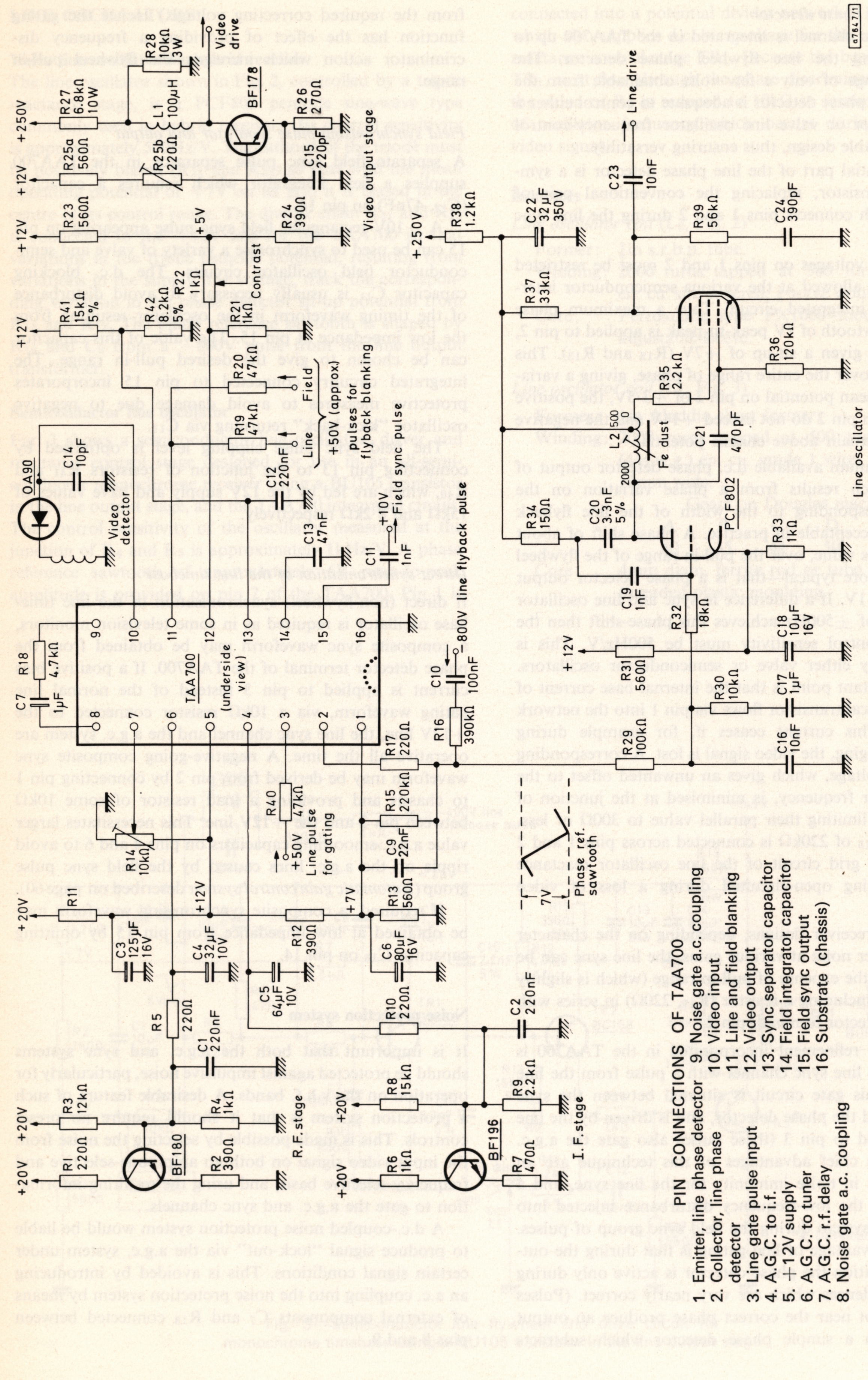
The a.g.c. system in the TAA700 is pulse-operated, therefore it is necessary to connect storage capacitors C_4 and C_5 to the a.g.c. output pins. These should be close to the TAA700 unit to restrict the path lengths of the pulse currents. Because of the sensitivity of a.g.c. leads to stray pick-up, particularly from the line timebase circuit, further decoupling is required: C_1 and R_5, and C_2 and R_{10}, placed close to the controlled stages. In a typical receiver layout with extended earthing connections for the tuner, the function of R_5 is especially important because it effectively raises the series impedance of the earth loop.

The line gating for the a.g.c. system (and also the line sync channel) is applied to pin 3 via R_{40}, and should have an amplitude between +1V and +5V.

Timebase synchronising system

Line sync pulse separator

The sync pulse separator function (with subsequent pulse clipping) is well suited to integrated circuit techniques. A conventional class C biased circuit requiring an external charge-storing capacitor, C_{12} on pin 13, has been adopted because of its self-adjusting properties during variations of signal level. It has been designed to have a fast reaction time so that sync is not disturbed during signal level fluctuations. The sync pulse separator is preceded by a low-pass filter (in the TAA700 unit) which suppresses h.f. noise.



+250V
R27 6.8kΩ 10W
R28 10kΩ 3W
Video drive
L1 100μH
R25a 560Ω
R25b 220Ω
BF178
R26 270Ω
C15 220pF
Video output stage
R23 560Ω
R24 390Ω
+12V
+5V
R22 1kΩ
Contrast
R41 15kΩ 5%
R42 8.2kΩ 5%
R21 1kΩ
R20 47kΩ
R19 47kΩ
Field
Line
+50V (approx) pulses for flyback blanking
OA90
C14 10pF
Video detector
C12 220nF
C13 47nF
C11 1nF
+10V Field sync pulse
800V line flyback pulse
R18 4.7kΩ
C7 1μF
TAA700 (underside view)
C10 100nF
R16 390kΩ
R17 220Ω
R15 220kΩ
R40 47kΩ
+50V Line pulse for gating
R14 10kΩ
C9 22nF
R13 560Ω
R11
+20V
+12V
+7V
C3 125μF 16V
C4 32μF 10V
R12 390Ω
C6 80μF 16V
C5 64μF 10V
R5 220Ω
C1 220nF
R10 220Ω
C2 220nF
R3 12kΩ
R4 1kΩ
R8 15kΩ
R9 2.2kΩ
R1 220Ω
R2 390Ω
R6 1kΩ
R7 470Ω
BF180
BF196
R.F. stage
I.F. stage
+250V
R38 1.2kΩ
C22 32μF 350V
C23 10nF
Line drive
R39 56kΩ
C24 390pF
R37 33kΩ
R36 120kΩ
R35 2.2kΩ
L2 500 2000
Fe dust
C21 470pF
PCF802
Line oscillator
R34 150Ω
C20 3.3nF 5%
R33 1kΩ
C19 1nF
R32 18kΩ
+12V
R31 560Ω
C18 10μF 16V
R30 10kΩ
C17 1μF
R29 100kΩ
C16 10nF
Phase ref. sawtooth
7V

PIN CONNECTIONS OF TAA700

1. Emitter, line phase detector
2. Collector, line phase detector
3. Line gate pulse input
4. A.G.C. to i.f.
5. +12V supply
6. A.G.C. to tuner
7. A.G.C. r.f. delay
8. Noise gate a.c. coupling
9. Noise gate a.c. coupling
10. Video input
11. Line and field blanking
12. Video output
13. Sync separator capacitor
14. Field integrator capacitor
15. Field sync output
16. Substrate (chassis)

Note: The value of R_{11} is determined by circuit considerations.

Fig. 2 TAA700 peripheral circuits for hybrid monochrome receiver

Line flywheel phase detector

The line sync channel is integrated in the TAA700 up to and including the line flywheel phase detector. The potential range of only a few volts obtainable from the line flywheel phase detector is adequate to control either a semiconductor or valve line oscillator frequency-control stage of suitable design, thus ensuring versatility.

The essential part of the line phase detector is a symmetrical transistor, replacing the conventional pair of diodes, which connects pins 1 and 2 during the line sync pulse.

Operating voltages on pins 1 and 2 must be restricted to the limits allowed at the various semiconductor interfaces of an integrated circuit. Thus a maximum phase reference sawtooth of 7V peak-to-peak is applied to pin 2, and pin 1 is given a sit-up of +7V (R_{12} and R_{13}). This ensures that over the entire range of phase, giving a variation of the mean potential on pin 2 of ±3·5V, the positive excursions on pin 2 do not exceed +14V and the negative excursions remain above chassis potential.

The maximum available d.c. phase detector output of ±3·5V (which results from a phase variation on the picture corresponding to the width of the line flyback pulse) is unacceptable in practice. A phase shift of about a third of this value, over the pull-in range of the flywheel system, is more typical—that is a phase detector output voltage of ±1V. If a difference in sync and line oscillator frequencies of ±500Hz achieves this phase-shift then the frequency control sensitivity must be 500Hz/V. This is easily met by either valve or semiconductor oscillators.

An important point is that the internal base current of the symmetrical transistor flows via pin 1 into the network R_{12}, R_{13}. This current ceases if, for example during channel changing, the video signal is lost. A corresponding change of voltage, which gives an unwanted offset to the line oscillator frequency, is minimised at the junction of R_{12}, R_{13} by limiting their parallel value to 300Ω or less. A resistor R_{15} of 220kΩ is connected across pins 1 and 2 to avoid the grid circuit of the line oscillator reactance stage becoming open-circuited during a loss of video signal.

In some receiver designs, depending on the character of the receiver noise at various gains, the line sync can be improved at the expense of pull-in range (which is slightly reduced) by including a resistor (R_{17}, 220Ω) in series with the phase detector terminal, pin 2.

A further refinement incorporated in the TAA700 is gating of the line sync channel with a pulse from the line timebase. This gate circuit is situated between the sync separator and the phase detector, and is driven by the line pulses applied to pin 3 (these pulses also gate the a.g.c. system). The chief advantages of this technique are an improvement in noise immunity for the line sync, and a reduction in the low-frequency disturbance injected into the flywheel system during the field sync group of pulses. A further advantage of line gating is that during the out-of-sync condition the phase detector is active only during phase coincidences which are very nearly correct. (Pulses which are not near the correct phase produce an output voltage from a simple phase detector which subtracts from the required correcting voltage.) Hence the gating function has the effect of providing a frequency discriminator action which increases the flywheel pull-in range.

Field synchronising pulse separator and output

A separate field sync pulse separator in the TAA700 supplies a field integrator which requires a capacitor (C_{13}, 47nF) on pin 14.

A +10V rectangular field sync pulse appearing on pin 15 can be used to synchronise a variety of valve and semiconductor field oscillator circuits. The d.c. blocking capacitor C_{11} is usually necessary to avoid disturbance of the timing waveform in the oscillator resulting from the low impedance at pin 15. The value of this capacitor can be chosen to give the desired pull-in range. The integrated circuitry connected to pin 15 incorporates protective measures to avoid damage due to negative oscillator "kick-back" returning via C_{11}.

The field sync pulse clipping level is optimised by connecting pin 13 to the junction of resistors R_{41} and R_{42}, which are fed by the 12V supply and have values of 15kΩ and 8·2kΩ respectively.

Direct synchronisation of the line timebase

If direct (non-flywheel) synchronisation of the line timebase oscillator is required as in some television monitors, a composite sync waveform may be obtained from the phase detector terminal of the TAA700. If a positive bias current is applied to pin 3 instead of the normal line gating waveform, via a 10kΩ resistor connected to the +12V line, the line sync channel and the a.g.c. system are operative all the time. A negative-going composite sync waveform may be derived from pin 2 by connecting pin 1 to chassis and providing a load resistor of some 10kΩ between pin 2 and the +12V line. This necessitates larger value a.g.c. smoothing capacitors on pins 4 and 6 to avoid ripple on the a.g.c. lines caused by the field sync pulse group (*Automatic gain control system* described on page 60).

If required, a composite synchronising waveform may be obtained at low impedance from pin 15 by omitting capacitor C_{13} on pin 14.

Noise protection system

It is important that both the a.g.c. and sync systems should be protected against impulsive noise, particularly for operation on the v.h.f. bands. A desirable feature of such a protection system is that it should require no preset controls. This is made possible by selecting the noise from the input video signal on both an amplitude-selective and frequency-selective basis, and using the resulting information to gate the a.g.c. and sync channels.

A d.c.-coupled noise protection system would be liable to produce signal "lock-out" via the a.g.c. system under certain signal conditions. This is avoided by introducing an a.c. coupling into the noise protection system by means of external components C_7 and R_{18} connected between pins 8 and 9.

LINE OSCILLATORS

Valve line oscillator for hybrid receiver

The line oscillator shown in Fig. 2, controlled by a triode reactance stage, is a PCF802 pentode sine-wave type commonly used in hybrid receivers. Its control sensitivity is approximately 500Hz/V. The cathode of the triode must be positively biased (R_{31} and R_{33}) so that with the mean operating potential of +7V on its grid it is biased in the centre of its control range. The divider chain R_{31} and R_{33} is connected to the +12V line for the TAA700 so that variations in the triode cathode potential, resulting from variations in the supply line voltage, track the corresponding variation in the phase detector sit-up potential from R_{12} and R_{13}. The phase reference sawtooth is shaped by R_{16} and C_9 from a −800V pulse from the line output transformer.

Semiconductor line oscillator

Fig. 3 shows a semiconductor line oscillator, driver and reactance control stage designed for use in an all-semiconductor monochrome receiver using a BU105 transistor in the line output stage, and the TAA700 integrated circuit. The control sensitivity of the oscillator measured at the junction of R_4 and R_5 is approximately 1kHz/V. A phase reference sawtooth of approximately 6V peak-to-peak amplitude is provided on pin 2 of the TAA700. Pin 1 is connected into a potential divider network R_1, R_2 and R_3 which also supplies d.c. bias voltage for the emitter of the reactance control stage TR_1. Because the base current for TR_1 must flow through the phase discriminator network, the value of R_8 is reduced to 10kΩ to minimise the drift of oscillator frequency which occurs during a loss of video signal.

Inductors

Line oscillator coil (L_2, Fig. 2)

Former: ¼in s.r.b.p. tube.
Winding: 2000 turns tapped at 500 turns, 42s.w.g. en. cu. silk covered, ¼-wave wound, ⅝in wide.
Core: Ferroxcube type FX1068 mounted in an adjustable sleeve.

Line oscillator coil (L_1, Fig. 3)

Former: ¼in Aladdin short former.
Winding: 2000 turns tapped at 500 turns, 0·08mm (44s.w.g.) en. cu. grade 1 wire, wave wound 10mm wide.

Gears on Douglas machine

A	B	C	D	E	F
40	35	44	50	24	96

Core: 4mm diam. ferrite rod or tube (FX1068) in threaded plastic moulding.

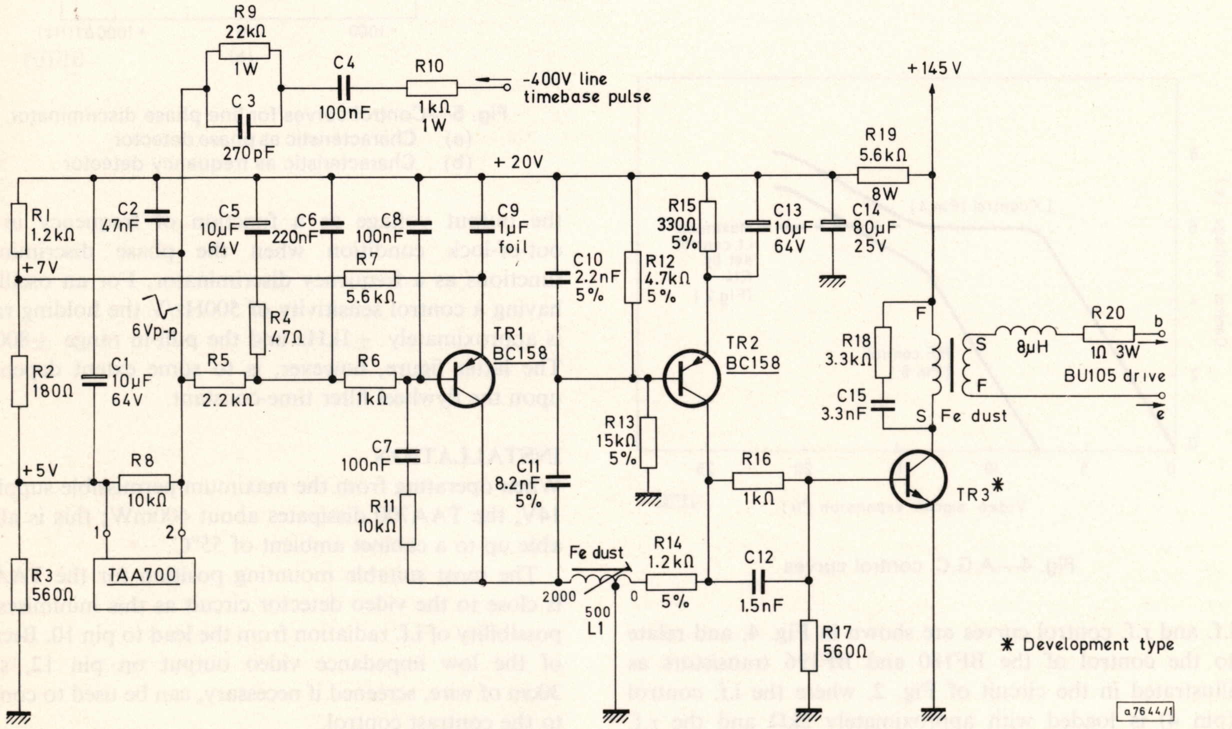


Fig. 3—Semiconductor line flywheel and drive circuit for monochrome timebase using a BU105 transistor in the line output stage

GENERAL PERFORMANCE OF THE TAA700

Nominal supply voltage	12V
Supply current nominal, no a.g.c.	22mA
max. demand	43mA
Total power dissipation ($T_{amb}=55°C$)	400mW
Operating ambient temperature range	−25 to + 55°C

Video amplifier development sample data

$V_{supply}=12V$, $R_{source}=0\Omega$, input from video detector =2V

Nominal output voltage (black-to-white value)	4·2V
Tolerances for above:	
Integrated circuit spreads	±375mV
Temperature	−14mV/degC
A.G.C. expansion (entire range)	±185mV

Nominal black level of output voltage	5V
Tolerances for above:	
Integrated circuit spreads	±400mV
Temperature	+7mV/degC
A.G.C. operation (entire range)	±250mV

The above figures apply to the following conditions:

1) Negative modulation of the signal is used in accordance with U.K. standards.
2) The a.g.c. is fully controlling the i.f. stage but not the r.f. stage.

A.G.C. system

The control of the i.f. amplifier stage starts as soon as the video input signal reaches a peak amplitude of 1·8V. The i.f. and r.f. control curves are shown in Fig. 4, and relate to the control of the BF180 and BF196 transistors as illustrated in the circuit of Fig. 2, where the i.f. control (pin 4) is loaded with approximately 2kΩ and the r.f. control (pin 6) with approximately 1kΩ. The i.f. control has been set to stop at +6V, and the maximum r.f. control is then +5V. Beyond this point both control outputs would begin to rise together. The video signal expansion on pin 10 over the normal a.g.c. control range is not greater than 15%.

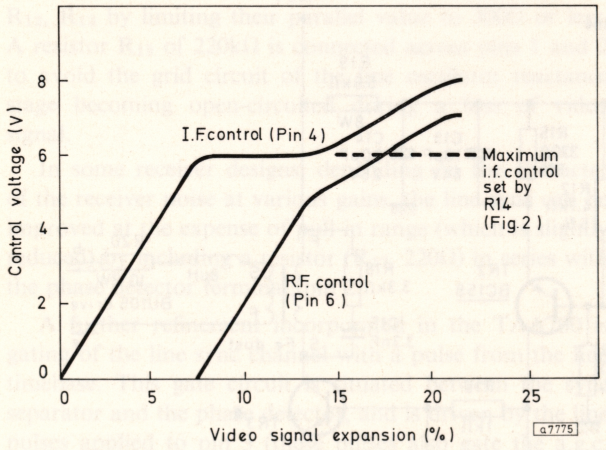


Fig. 4—A.G.C. control curves

Synchronising system

The control curves for the line phase discriminator depend mainly upon the amplitude of the phase reference waveform, and the width of the line flyback pulse from which it is derived. Fig. 5a shows the control voltage output as a function of phase error, given in microseconds and related to a line flyback pulse duration of approximately 12μs, over the phase locked region. Fig. 5b shows the output voltage as a function of frequency in the out-of-lock condition when the phase discriminator functions as a frequency discriminator. For an oscillator having a control sensitivity of 500Hz/V the holding range is approximately ±1kHz and the pull-in range ±800Hz. The latter figure, however, is to some extent dependent upon the flywheel filter time-constant.

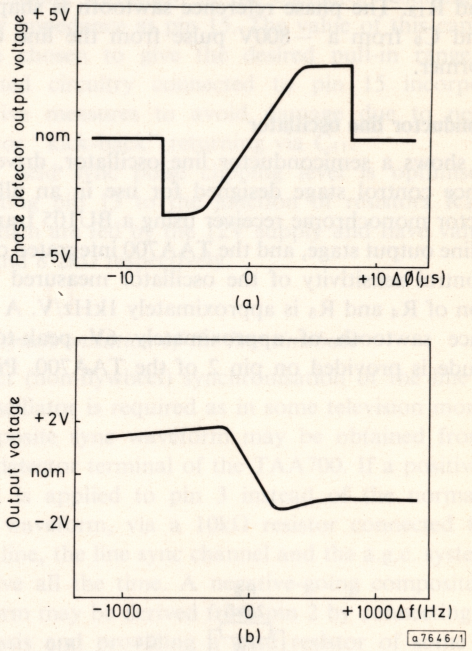


Fig. 5—Control curves for line phase discriminator
(a) Characteristic as phase detector
(b) Characteristic as frequency detector

INSTALLATION

When operating from the maximum permissible supply of 14V, the TAA700 dissipates about 400mW; this is allowable up to a cabinet ambient of 55°C.

The most suitable mounting position for the TAA700 is close to the video detector circuit as this minimises the possibility of i.f. radiation from the lead to pin 10. Because of the low impedance video output on pin 12, some 30cm of wire, screened if necessary, can be used to connect to the contrast control.

Careful positioning of the decoupling capacitors is essential because of the high power gain, common to many integrated circuits, of the TAA700. All external capacitors intended for decoupling points on the integrated circuit unit should, as a general rule, be mounted as close to the unit as possible and have direct returns to substrate (chassis), pin 16. This applies to components C_3, C_4, C_5, C_6, C_{12} and C_{13} (Fig. 2).

The importance of adequate decoupling on the a.g.c. control connections, pins 4 and 6, has already been discussed. The effect of inadequate decoupling is usually the appearance of line pulses on the detected video waveform, and this can seriously impair the field interlace. Attention to adequate decoupling of all the tuner and i.f. d.c. connections usually prevents this, and only in difficult receiver layouts has it been necessary to screen the a.g.c. leads.

The precautions normally taken in receivers using semiconductor devices should adequately protect the TAA700 from picture tube flashover. However, if the tuner and video contrast controls are on the front of the receiver, their mountings and connections need attention to avoid possible arcing between the picture tube rimband and the integrated circuit.

The 16-lead 'quad-in-line' layout has been adopted for the TAA700 to facilitate its use with printed panels by giving adequate distance between the pin centres. The circuit may either be soldered into a printed board or used with plug-in holder.

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Decoding circuits with colour-difference output

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Decoding circuits are described for the colour-processing area of a delay-line PAL colour receiver operating with colour-difference drive to the picture tube. Silicon transistors are used in the chrominance amplifier, subcarrier regenerator and phase-switching stages. Automatic chrominance gain control is used to reduce the effects of a varying luminance-chrominance ratio resulting from transmission and fine-tuning errors.

INTRODUCTION

The article describes a complete decoding system for the colour processing area of a single-standard, delay-line PAL colour receiver. The decoding circuits accept chrominance information from the vision i.f. amplifier and, after processing, provide colour-difference output signals.

The chrominance amplifier has been designed to work into an ultrasonic glass delay-line to provide PAL-D decoding and demodulation. The delay-line has the exact delay (63·943μs).

Phase switching on alternate lines is achieved by the use of a diode switch controlled by a bistable circuit. The system is driven from the line timebase; the phase of switching is checked by reference to the swinging colour burst.

DECODER

The decoder is best explained initially by reference to the block diagram, shown in Fig. 1, which gives the general layout of the circuit diagram of Fig. 2. There are two main paths through the system, the reference path and the chrominance path. These diverge from the two common stages at the left-hand side of Fig. 1.

Initially, the chrominance signal is extracted from the composite detected signal by the chroma take-off network which feeds the controlled chrominance amplifier. Automatic chrominance control (a.c.c.) is applied to this stage to maintain a constant reference colour-burst amplitude, and to provide a constant source of chrominance signal.

The reference path at the top of the diagram in Fig. 1 shows that the complete chrominance signal is amplified in the first colour-burst amplifier which feeds the burst-gate amplifier, and this in turn drives the reference phase detector. A sample of the burst signal is taken to the a.c.c. detector for control purposes.

The phase detector produces a d.c. signal by phase-sensitive detection of the swinging colour-burst signal. The d.c. control signal is smoothed by the low-pass filter, which is included to control the pull-in characteristics and reduce the effects of noise. After d.c. amplification, the d.c. signal is used to control the variable-capacitance diode which, in turn, controls the phase of the crystal oscillator.

The residual 7·8kHz ripple from the detector is employed to drive a phase-checking circuit consisting of a tuned 7·8kHz amplifier and emitter-follower which also drives a 'colour-killer' bias circuit. An economy in components has been achieved by combining the function of phase checking with that of colour killing when monochrome transmissions are received.

The reference signal from the crystal oscillator is distributed by an emitter-follower buffer stage to the phase detector, the 90° phase shifter and the subcarrier phase switch (PAL bistable switch).

The chrominance signal path, shown below the reference path, starts at the saturation (chroma gain) control which determines the proportion of the a.c.c. controlled signal fed into the chroma amplifier proper. A delay-line driver amplifier is employed to provide both a high-impedance current source for the delay-line, which is terminated at the sending end by a 100Ω resistor, and an undelayed signal for the separator network.

Following the delay-line circuit, the (R-Y) and (B-Y) components of the chrominance signal are separated and fed to two diode-bridge synchronous demodulators. After passing through low-pass filters which remove the subcarrier frequency, the colour-difference signals drive a pair of transistors from which the (G-Y) signal is obtained by emitter matrixing. The three signals thus obtained are used to base drive the colour-difference output stages, the picture tube grids being a.c. coupled and clamped by double-diode clamps. Details of the matrix and output stages are given in Ref. 1.

CHROMINANCE AMPLIFIER

Chrominance take-off circuit

The chrominance signal is obtained from a separate detector D_{101} etc. in Fig. 2, which supplies only the sound and chroma circuits. The chroma signal is separated from the composite signal on this detector by high-pass filter L_{117}, C_{134} and L_{119}, the sound carrier being attenuated some 3dB by the sound take-off transformer L_{116} and L_{115}. The full circuit of the sound/chroma detector and chroma take-off also appears in Ref. 2.

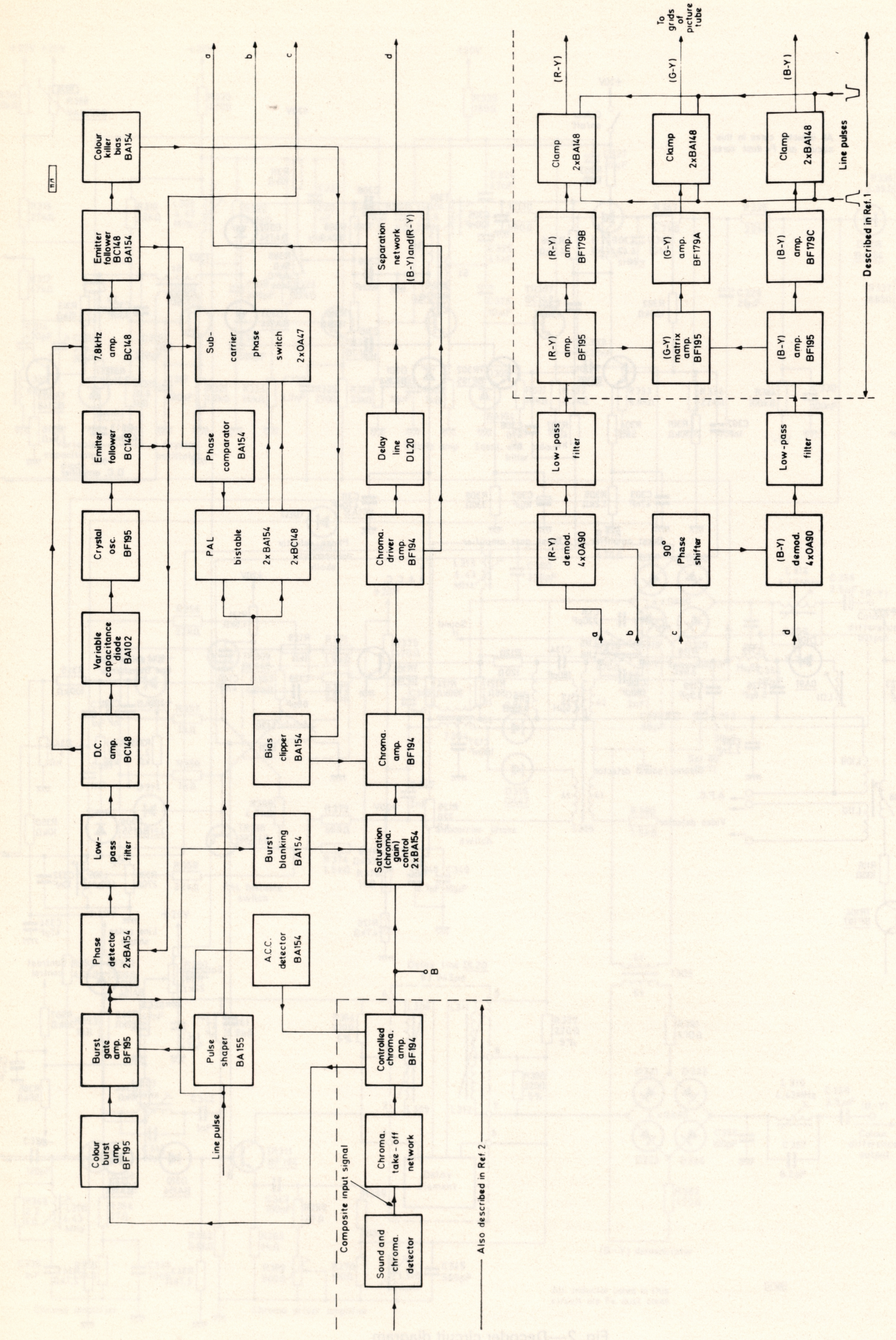
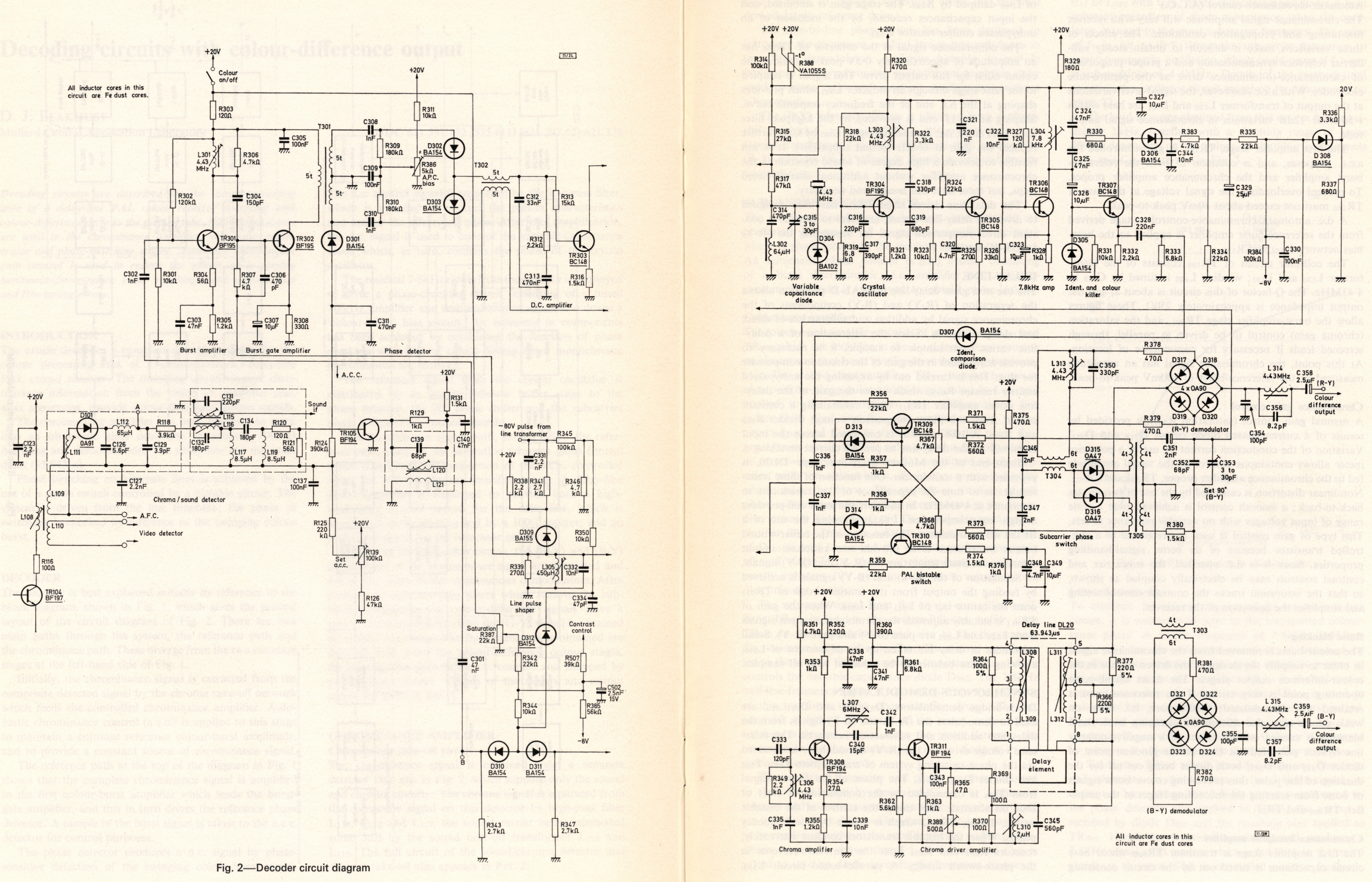

Colour burst amp. BF195
Burst gate amp. BF195
Phase detector 2xBA154
Low-pass filter
D.C. amp. BC148
Variable capacitance diode BA102
Crystal osc. BF195
Emitter follower BC148
7·8kHz amp. BC148
Emitter follower BC148 BA154
Colour killer bias BA154
Pulse shaper BA155
Line pulse
A.C.C. detector BA154
Burst blanking BA154
Bias clipper BA154
PAL bistable 2xBA154 2xBC148
Phase comparator BA154
Sub-carrier phase switch 2xOA47
Sound and chroma detector
Composite input signal
Chroma. take-off network
Controlled chroma. amp. BF194
Also described in Ref. 2
Saturation (chroma. gain) control 2xBA154
Chroma. amp. BF194
Chroma. driver amp. BF194
Delay line DL20
Separation network (B-Y)and(R-Y)
B
a
b
c
d
(R-Y) demod. 4xOA90
90° Phase shifter
(B-Y) demod. 4xOA90
Low-pass filter
Low-pass filter
(R-Y) amp. BF195
(G-Y) matrix amp. BF195
(B-Y) amp. BF195
(R-Y) amp. BF179B
(G-Y) amp. BF179A
(B-Y) amp. BF179C
Clamp 2xBA148
Clamp 2xBA148
Clamp 2xBA148
Line pulses
Described in Ref. 1
(R-Y)
(G-Y)
(B-Y)
to grids of picture tube

Fig. 1—Block diagram of decoder



All inductor cores in this circuit are Fe dust cores.
Colour on/off
Burst amplifier
Burst gate amplifier
Phase detector
A.P.C. bias
D.C. amplifier
A.C.C.
Chroma/sound detector
Sound if
A.F.C.
Video detector
−80V pulse from line transformer
Line pulse shaper
Set a.c.c.
Saturation
Contrast control
Variable capacitance diode
Crystal oscillator
7.8kHz amp
Ident. and colour killer
Ident. comparison diode
PAL bistable switch
Subcarrier phase switch
(R−Y) demodulator
(B−Y) demodulator
Colour difference output
Set 90°
Delay line DL20 63.943µs
Delay element
Chroma amplifier
Chroma driver amplifier

Fig. 2—Decoder circuit diagram

Automatic-chrominance-control (A.C.C.)

The chrominance signal amplitude will vary with receiver fine-tuning and propagation conditions. The effects of these variations make it difficult to obtain steady subcarrier reference synchronisation and a proper proportion of chrominance-to-luminance drive at the picture-tube electrodes. With a.c.c., however, the signal-level variations at the output of transformer L$_{120}$ and L$_{121}$ are held within 1·5dB for 12dB variations in chrominance signal amplitude.

The first amplifier stage, TR$_{105}$, is gain-controlled for a.c.c. purposes, and is common to both the reference-burst amplifier and the chrominance amplifier proper. To prevent overloading, the signal voltage at the base of TR$_{105}$ must not exceed about 30mV peak-to-peak.

A d.c. automatic-chrominance-control voltage derived from the reference-burst amplifier is applied to the base-bias network R$_{124}$ and R$_{125}$.

The collector circuit of TR$_{105}$ consists of the transformer L$_{120}$ and L$_{121}$; winding L$_{120}$ is tuned by C$_{139}$ to 4·43MHz. The Q-factor of this circuit is about 2, and the output impedance is approximately 250Ω. These figures allow the burst-amplifier stage TR$_{301}$, and the saturation (chroma gain) control to be driven in parallel, through screened leads if necessary for convenience of location. At this point, the chrominance signal has an amplitude measured at the reference-burst of 100mV peak-to-peak.

Chrominance gain control

A manual gain control (saturation R$_{387}$) is provided by means of a current-biased diode circuit D$_{310}$ and D$_{311}$. Variation of the conduction current by use of a potentiometer allows continuous control of the signal amplitude fed to the chrominance amplifier proper, TR$_{308}$ and TR$_{311}$. Non-linear distortion is cancelled by the use of two diodes back-to-back; a smooth control is achieved over a wide range of input voltages with no variable reactance effects. This type of gain control is used in preference to a controlled transistor because of its better signal-handling properties. Since it is d.c. operated, the subcarrier and contrast controls may be electrically coupled as shown, so that the saturation tracks the contrast control setting and simplifies the operation of the receiver.

Burst blanking

The colour-burst is removed from the chrominance signal in order to simplify the design of the driven clamps in the colour-difference output stages. The exact clamp-pulse operating point is very critical if the reference burst is retained and demodulated; furthermore, h.f. noise on weak signals may also disturb the clamping level. Burst blanking is carried out by means of a negative-polarity line flyback pulse fed via D$_{312}$ to the junction point of diodes D$_{310}$ and D$_{311}$, both diodes being cut off for the duration of line pulse, thus preventing colour-burst signals or noise from entering the succeeding stages of the amplifier, TR$_{308}$ and TR$_{311}$.

Chrominance bandpass amplifier

The first amplifier stage is transistor TR$_{308}$ whose base circuit capacitance is tuned out by the circuit consisting of L$_{306}$ damped by R$_{349}$. The stage gain is stabilised, and the input capacitances reduced, by the inclusion of an unbypassed emitter resistor R$_{354}$.

The chrominance signal at the collector of TR$_{308}$ has an amplitude of approximately 0·5V peak-to-peak at the colour-burst for full output drive. This signal is coupled to the next stage through an inductor L$_{307}$ which provides shaping at the h.f. end of the frequency-response curve. Shaping at the l.f. end is provided by the highpass filter L$_{117}$, L$_{119}$ and C$_{134}$; parallel tuning of L$_{307}$ by C$_{340}$ further reduces the gain at 6MHz (sound subcarrier). It is not feasible to provide a high degree of sound rejection in the chrominance amplifier without additional sharply-tuned traps, but these have not been found necessary.

The delay-line driver stage TR$_{311}$ has been designed to drive the delay-line circuit, and also to provide a constant direct-comparison signal for separating the (R-Y) and (B-Y) signals.

DELAY-LINE

The use of a glass delay-line for PAL-D reception allows the separation of (R-Y) and (B-Y) components of the chrominance signal by addition and subtraction of direct and delayed signals. Since the attenuation of a delay-line varies from sample to sample, it is necessary to provide adjustment in the gain of the circuit to compensate for this. This is carried out by adjusting the unbypassed emitter resistor R$_{389}$, which varies the gain of the delay-line driver amplifier TR$_{311}$ while maintaining a constant output from the direct-comparison voltage divider R$_{369}$ and R$_{370}$. A 100Ω resistor is connected across the input terminals of the delay-line to provide correct matching.

Each end of the Mullard delay-line, type DL20, is provided with a transformer. One function of these transformers is to tune the capacitance of the transducers to resonance at 4·43MHz. In addition, the input coil provides a high input impedance (1·6kΩ) allowing the use of a BF194 driver transistor. The function of the bifilar-wound output transformer is to provide two antiphase output signals to facilitate separating the (R-Y) and (B-Y) signals.

Separation of the (R-Y) and (B-Y) signals is achieved by feeding the output from the emitter circuit of TR$_{311}$ onto the centre tap of L$_{311}$ and L$_{312}$. When the gain of TR$_{311}$ is suitably adjusted, the chrominance output signals from L$_{311}$ and L$_{312}$ are pure (B-Y) and pure (R-Y). Small tolerances in delay are taken up by adjustment of L$_{310}$, allowing phase balance to be achieved with all samples.

SYNCHRONOUS DEMODULATION

Diode-bridge demodulators, D$_{317-320}$ and D$_{321-324}$, are used to demodulate the (R-Y) and (B-Y) signals from the delay-line addition and subtraction networks. The reference voltage drive for the (R-Y) demodulator is obtained via the phase-switching system of transformers T$_{304}$, T$_{305}$ and diodes D$_{315}$, D$_{316}$. The phase of the output signal from T$_{304}$ is determined by the conduction of D$_{315}$ or D$_{316}$ on alternate lines under the control of the bistable switch, TR$_{309}$, TR$_{310}$, which is driven by line frequency pulses. When the bistable transistors conduct alternately, resistors R$_{372}$ and R$_{373}$ limit the 'turn-on' currents in the phase-switch diodes. A parallel-tuned circuit L$_{313}$, C$_{350}$ is used to remove harmonics from the switched demodulation-reference drive.

The line-by-line phase-switch has been designed to introduce the minimum residual line-to-line unbalance in the (R-Y) demodulator. A driven bistable is used in preference to a synchronised multivibrator to obtain unity mark-to-space ratio and constant synchronism without adjustments.

The (B-Y) reference voltage is obtained from a phase-shift network C$_{352}$, C$_{353}$ and R$_{380}$, driven from the centre-tapped transformer T$_{305}$. The 90° phase-shift between the (R-Y) and the (B-Y) reference signals is adjusted by the trimmer C$_{353}$.

SUBCARRIER REGENERATOR

The reference signals for synchronous demodulation are generated by means of a crystal-controlled oscillator which is phase-locked to the received colour-burst signal. An automatic phase control (a.p.c.) system consisting of a burst discriminator, d.c. amplifier and variable-capacitance diode is employed to obtain phase-locking.

Colour-burst amplifier

The colour-burst amplifier consists of transistors TR$_{301}$ and TR$_{302}$ which are included in the a.c.c. loop, thus ensuring an almost constant burst amplitude at the phase discriminator. The second-stage transistor TR$_{302}$ is gated by means of a positive-going pulse which is generated in L$_{305}$ and applied to the base resistor R$_{307}$. Differentiated line pulses from C$_{331}$ and R$_{341}$ are applied to the ringing circuit L$_{305}$ and C$_{332}$ via diode D$_{309}$. At this point they generate an initial negative pulse of about 5V followed by an overswing pulse of about 3V amplitude which coincides with the colour-burst. It is the overswing pulse which gates the burst. The secondary winding of the phase-splitting transformer T$_{301}$ is connected to the phase-discriminator diodes D$_{302}$ and D$_{303}$, and also to the a.c.c. rectifier D$_{301}$. The a.c.c. voltage generated at the anode of D$_{301}$ is used to control the variable-gain chrominance take-off stage TR$_{105}$ via R$_{124}$, maintaining an approximately constant 10V peak-to-peak burst voltage at the discriminator diodes.

The reference signal from the crystal-controlled oscillator TR$_{304}$ is fed via the emitter-follower buffer stage TR$_{305}$ to the demodulator, and also to the burst-phase discriminator via transformer T$_{302}$. Phase error signals are fed to the base of the d.c. amplifier transistor TR$_{303}$ which controls the variable-capacitance diode D$_{304}$. The 7·8kHz half-line-frequency signal is also taken from the collector of this transistor to the phase-identity circuit. The d.c. amplifier is biased by means of the preset control R$_{386}$ so that, with zero output from the phase detector, the reverse bias on the variable-capacitance diode is in the correct operating region.

The oscillator frequency and phase are then adjusted to the correct value by means of C$_{315}$. The additional trimmer and inductor across the variable-capacitance diode are included to enable a wide spread of diode capacitance to be employed without the need to change padding capacitors. It can be shown that if L$_{302}$ is fixed, and C$_{315}$ is varied to take up diode spreads, the resonant frequency (f$_1$) of L$_{302}$ with C$_{315}$, diode capacitance and strays is held constant regardless of diode capacitance, when the oscillator is tuned to the exact subcarrier frequency. The value of f$_1$ is set at 0·7 times the subcarrier frequency to avoid parametric oscillation, which could occur if f$_1$ were a sub-multiple of 4·4MHz. Details of the method used to set-up the oscillator circuit are given in *Adjustments* on page 72.

The hold-in range obtained from this system is approximately 1kHz, together with a catching range of some 500Hz dependent on the values of the filter components R$_{312}$ and C$_{313}$ as shown in Fig. 3.

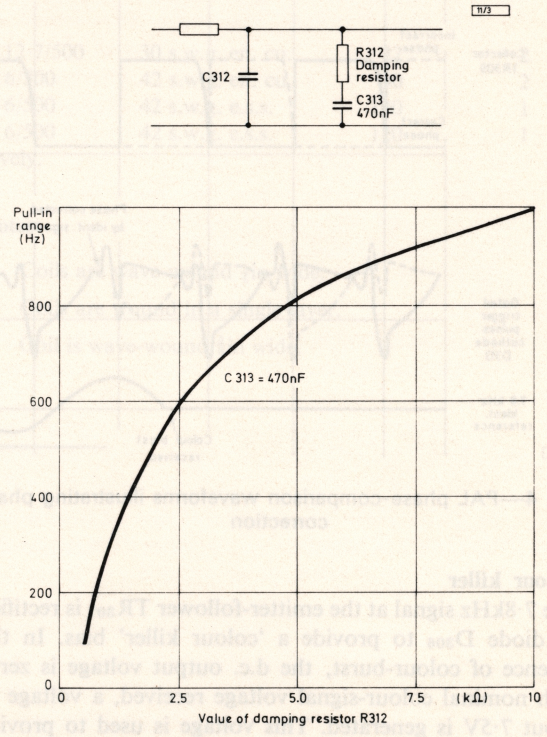


Fig. 3—A.P.C. loop pull-in characteristics

Line phase-identity

To establish the correct phasing of the reference switch circuit, it is necessary to refer to the transmitted colour-burst phase. A switch frequency of 7·8kHz (half-line-frequency) for the reference waveform is obtained by amplifying the swinging burst ripple which is present at the collector of the d.c. amplifier TR$_{303}$ in the subcarrier regenerator circuit. A tuned amplifier TR$_{306}$ is used to reduce the effects of noise during the colour-burst period. The tuned circuit is formed by the inductor L$_{304}$ and capacitors C$_{324}$ and C$_{325}$; the effective Q-factor is improved by positive feedback from the emitter-follower TR$_{307}$.

Transistor TR$_{307}$ is not provided with any base bias and, therefore, in the absence of the 7·8kHz signal, its current is zero. When the 7·8kHz signal is generated by the phase detector and applied to TR$_{306}$, the output is rectified by diode D$_{305}$ and the resulting bias applied to TR$_{307}$. Hence the transistor conducts, and produces a 7·8kHz signal at its emitter which is fed back to the tuned circuit at its input. This is controlled positive feedback, and a large-amplitude 7·8kHz signal is produced at the emitter of TR$_{307}$. Switch-phase comparison is carried out by the components D$_{307}$, R$_{333}$ and C$_{328}$ which modify the operation of the switch steering circuit R$_{356}$ and D$_{313}$. In correct phase operation, the triggering of the bistable is not affected, but if the phase is wrong the driving pulse through C$_{336}$ is suppressed by the blocking bias through D$_{307}$. Phase-comparison waveforms are shown in Fig. 4.

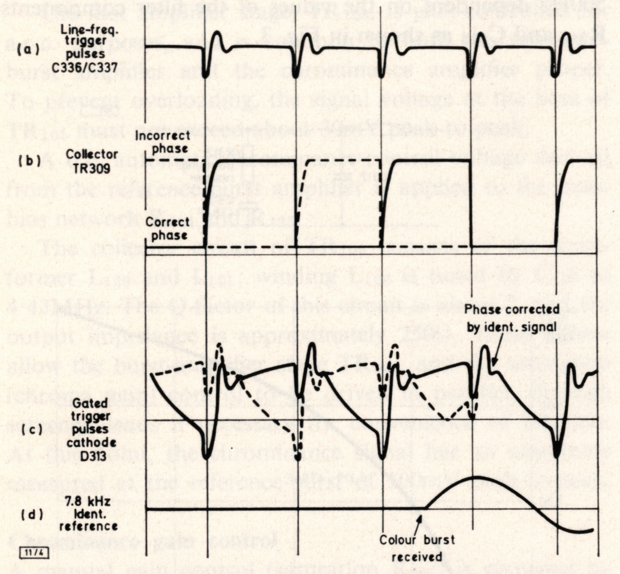


Fig. 4—PAL phase-comparison waveforms illustrating phase correction

Colour killer

The 7·8kHz signal at the emitter-follower TR$_{307}$ is rectified by diode D$_{306}$ to produce a 'colour killer' bias. In the absence of colour-burst, the d.c. output voltage is zero; with nominal colour-signal voltage received, a voltage of about 7·5V is generated. This voltage is used to provide a turn-on bias for the chrominance amplifier TR$_{308}$ after smoothing by R$_{335}$ and C$_{330}$, and clipping by D$_{308}$. A small negative voltage is applied at the anode of D$_{308}$ to ensure that the 'colour killer' operation is satisfactory when receiving noisy monochrome signals.

REFERENCES

1. Gander, M. C. and Hampson, L., 'Luminance, colour-difference output, synchronising and a.g.c. circuits', **Mullard Technical Communications**, Vol. 11, No. 102, Nov. 1969, pp. 35 to 45.
2. Bissmire, P., 'Single system i.f. amplifier for U.K. 625-line system', **Mullard Technical Communications**, Vol. 10, No. 98, Mar. 1969, pp. 234 to 243.
3. Hobbs, D. S., 'Hybrid colour-difference decoding circuits', **Mullard Technical Communications**, Vol. 9, No. 85, Jan. 1967, pp. 111 to 118.

APPENDIX 1

Adjustments

Crystal oscillator

After tuning L$_{303}$ for maximum reference output on TR$_{305}$ emitter, and with a colour-burst present, unplug the crystal. Connect a d.c. voltmeter (Avometer model 8, 25V range) between the collector of TR$_{303}$ and chassis, and adjust R$_{386}$ to give a reading of 6V. Reconnect the crystal, and adjust C$_{315}$ to restore colour synchronism, continuing the adjustment until the voltmeter again reads 6V. This places the operating point of the variable-capacitance diode in the correct region for good hold-in and pull-in characteristics.

Delay-line

If possible, apply a colour-bar signal with normal PAL burst but with the (R-Y) signal unswitched (that is, the picture information NTSC coded). Adjust R$_{387}$ (amplitude) and L$_{310}$ (phase) to give minimum output from the (R-Y) demodulator. If the burst phase is also unswitched, the same method may be used, but the 'colour killer' must be disabled.

If a suitable generator is not available, then the method outlined in Ref. 3 should be used:

With the subcarrier oscillator locked to an incoming signal, feed the unmodulated reference signal from the emitter of TR$_{305}$ into the saturation control (point 'B' on Fig. 2) in place of the normal signal, and adjust R$_{387}$ and L$_{310}$ for minimum (R-Y) output. This should be determined by an oscilloscope connected to the appropriate pin on the delay-line.

Subcarrier phase-shift

With a normal colour-bar input, short-circuit the delay-line input, effectively converting the decoder to PAL-S. Adjust L$_{301}$, if required, to provide minimum difference between adjacent lines of (R-Y) information as observed on an oscilloscope, or as minimum 'Hanover bars' on the red gun of the picture tube. Adjust C$_{353}$ for a similar balance with the (B-Y) signal (or blue gun). The two adjustments will interact slightly, so the (R-Y) signal should be checked again if a large adjustment is needed.

General adjustments

Adjustment of the subcarrier phase-shift and delay-line balance may be carried out conveniently by using a Philips pattern generator type PM5508. This generator, in the 'delay' position, provides a signal which has PAL burst and NTSC colour-difference modulation. This will cause 'Hanover bars' to be produced in the event of delay-line unbalance, and the modulation used facilitates discrimination between amplitude and phase unbalance.

In the 'phase' position, a colour-bar pattern of 50% saturation is displayed in the upper half of the picture, and in the lower half is the same pattern at 100% saturation but with colour-difference information only on 'even' lines. The effect is that the lower half is demodulated in the same way as NTSC and, in the presence of phase errors in the reference path, hue errors will be observed when the two halves of the picture are compared.

APPENDIX 2

Transformers

All cores are type FX2249, and all windings are of 38 s.w.g. t.n.a.

Transformer	Location	Primary turns	Secondary turns
T$_{301}$	Phase detector	5	5+5 bifilar
T$_{302}$	Phase detector	5	5
T$_{303}$	(B-Y) ref.	4	6
T$_{304}$	(R-Y) ref.	6	6
T$_{305}$	(R-Y) switch	4+4 bifilar	4+4 bifilar

Inductors

Inductor	Location	Former	Core	Wire	No. of turns	Note
L$_{120}$ L$_{121}$	A.C.C. output	P1011/1	4×0·5×6/900	42 s.w.g. t.n.a.	50 25	1
L$_{301}$	Burst amp.	P1011/1	4×0·5×6/500	42 s.w.g. en. cu.	55	2
L$_{302}$	Crystal osc.	CH1/1		42 s.w.g. en. cu.	51	2
L$_{303}$	Crystal osc.	P1011/1	4×0·5×6/500	42 s.w.g. en. cu.	30	2
L$_{304}$	Ident. coil	8A-6030-01	6×1×12·7/100	42 s.w.g. en. cu.	1700	3
L$_{305}$	Burst gate pulse	P1011/1	4×0·5×12·7/500	42 s.w.g. e.s.s.	250	1
L$_{306}$	Chroma. amp.	P1011/1	4×0·5×6/500	42 s.w.g. e.s.s.	80	1
L$_{307}$	Chroma. amp.	P1011/1	4×0·5×6/500	42 s.w.g. e.s.s.	65	1
L$_{308}$ L$_{309}$ L$_{311}$ L$_{312}$	Built into DL20 delay-line					
L$_{310}$	Delay-line bal.	P1011/1	4×0·5×12·7/500	30 s.w.g. en. cu.	22	2
L$_{313}$	(R-Y) ref. out.	P1011/1	4×0·5×6/500	42 s.w.g. en. cu.	30	2
L$_{314}$	Output filter	P1011/1	4×0·5×6/500	42 s.w.g. e.s.s.	120	1
L$_{315}$	Output filter	P1011/1	4×0·5×6/500	42 s.w.g. e.s.s.	120	1

Capacitors C$_{356}$ and C$_{357}$ are in the same cans as L$_{314}$ and L$_{315}$ respectively.
CH1/1 is a dust iron choke made by Neosid.

Formers

P1011/1 is made by E.I.H. Electronics Limited, and is $\frac{3}{16}\times\frac{3}{4}$in.
8A-6030-01 is made by Aladdin, and is 0·3in diameter.

Cores

All cores are Neosid; grade 900, 500 or 100.

Notes

1. Coils are wave-wound $\frac{1}{4}$in wide.
2. Coils are wound in a single layer.
3. Coil is wave-wound $\frac{3}{8}$in wide.

Mullard Technical Handbook

Mullard data sheets are now available in new format: bound volumes have replaced the earlier ring binders which held loose data sheets. The Mullard Technical Handbook of data on components recommended for new equipment design now consists of fourteen such volumes which are grouped and labelled as parts of three main 'books'. Book 1 contains the data for semiconductor devices (including integrated circuits) and has six parts—or six volumes. Book 2 contains the data for valves and tubes and has five parts. Book 3 contains the data for passive components and materials and has three parts.

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Finding a wanted data page is made easy in the new format. First, a 'quick-reference thumb guide' is incorporated into the contents page and the page edges, so that sections can be located very rapidly. Second, there is an alpha-numerical index in each part, so that if the required type-number is known the wanted data can be found directly. Third, a well planned selection-guide is included in each volume, so that if the application for the component can be specified then all the likely component types and data pages are indicated immediately.

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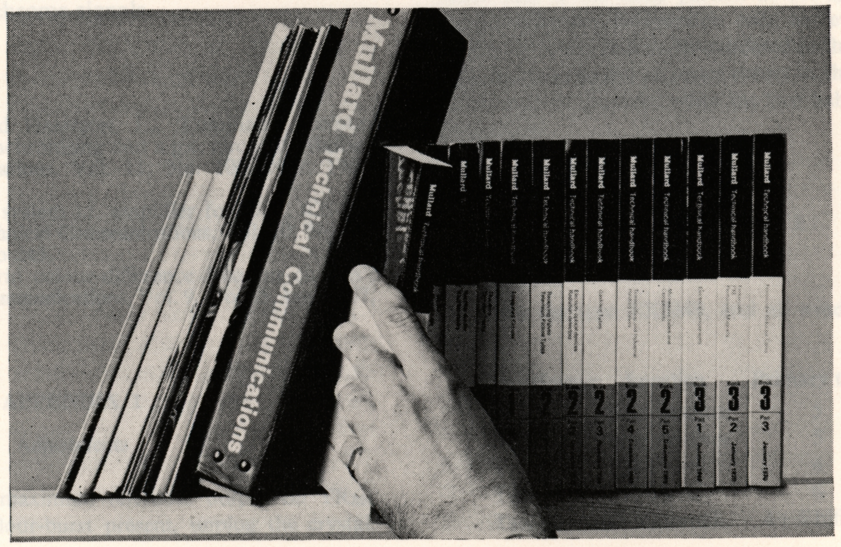

Dynamic stability of thyristor single-phase motor speed-control systems for d.c. shunt machines

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UDC 621.316.718.016.352:621.313.223:621.382.333.4

An investigation into the dynamic stability of thyristor motor speed-control systems is described. Measurements were made on the Mullard tachometer and armature-voltage feedback systems, which were found to be suitable for use with all normal power-absorbing or high-inertia mechanical loads, and with normal shunt motors which are used on single-phase a.c. supplies. The armature-voltage feedback system, however, may only just be stable with certain motors and loads, and an improved circuit which uses an alternative filter is recommended. The same filter circuit may also be used with the tachometer system. The performance of this system with the improved filter is similar to that of the published circuit, with the exception that the speed overshoot following a large transient load is considerably reduced because of the reduction of stored charge and smaller voltage excursion across the filter capacitors.

INTRODUCTION

It is often thought that the stability of a closed-loop control system is always a complicated problem involving complex mathematical analysis. This is not necessarily so. In some cases, of course, stability is complicated, and the conditions for it difficult to assess. In other cases, the whole problem can virtually be reduced to a simple set of rules that will cover almost every situation in which the system will be required to operate. This simple approach can be applied to the tachometer and armature-voltage feedback motor speed-control systems described in Refs. 1 and 2.

A number of different stability conditions must be satisfied before any control system will operate effectively. In the case of the motor speed-control systems under consideration, it is usual to specify the change in speed for a change in load torque, supply voltage, and ambient temperature. These are normally relatively slowly changing variables, and the low-frequency or steady-state conditions are given in the specifications. Sometimes, however, the load torque may change rapidly and it is useful to know the system response time under these conditions.

It is also essential to establish that a closed-loop control system is dynamically stable, and to define the limits of stable operation. The theory of closed-loop feedback systems and conditions for dynamic stability are extensively documented elsewhere (Ref. 3). This investigation presents the dynamic gain and phase shift measurements made on the tachometer and armature-voltage feedback motor speed-control systems, and discusses the relationship between these results and practical circuit designs.

The speed-control systems under consideration consist of three principal active parts: the motor and associated mechanical load, the speed-measuring tachometer or bridge, and the feedback amplifier. Each part produces some phase shift so that it is possible for the overall system gain to exceed unity at a phase shift of 180°; that is for the Nyquist plot of gain and phase to enclose the point $(-1, 0)$. This is the well-known condition for system instability, and operation in this region must be avoided.

The transfer functions (gain/phase characteristics) of the speed-control systems can be measured over a wide frequency range with different motor loads and with different filter networks in the feedback circuit. These results can give an insight into the operation of the circuits which makes it possible to modify the design to some extent if necessary to improve the degree of stability.

MEASURING TECHNIQUES

Measurements were made on the tachometer and armature-voltage feedback speed-control systems, the circuit diagrams for which are shown in Figs. 7 and 11 of Ref. 1,

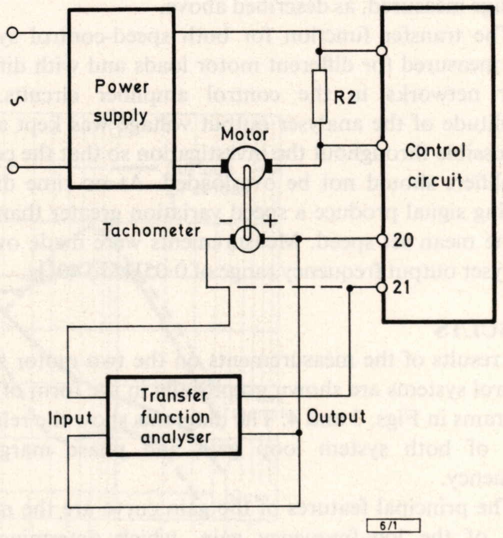

Fig. 1—Transfer function analyser connected to tachometer system

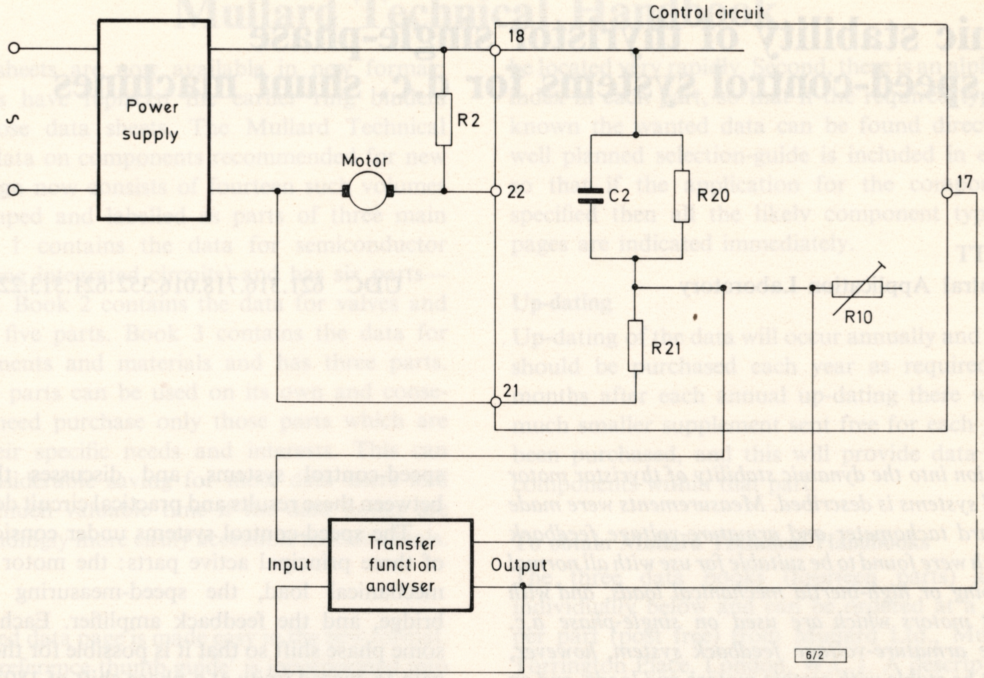

Fig. 2—Transfer function analyser connected to armature-voltage system

and the circuit diagrams of Ref. 2. The component references are the same for all the diagrams.

In the tachometer system, the feedback loop was broken at terminal 21 and a transfer function analyser connected as shown in Fig. 1. The analyser supplied a sinusoidal voltage signal to the control circuit to simulate an error signal from the tachometer. The output voltage from the tachometer was fed into the analyser, which indicated the voltage gain round the loop and the phase shift between the input and output voltages.

In the armature-voltage feedback system, the feedback loop was broken at the feedback bridge end of resistor R_{10} and the transfer function analyser connected as shown in Fig. 2. A simulated error signal was applied and the output voltage measured, as described above.

The transfer function for both speed-control systems was measured for different motor loads and with different filter networks in the control amplifier circuits. The amplitude of the analyser output voltage was kept as low as possible throughout the investigation so that the control amplifiers should not be overloaded. At no time did the driving signal produce a speed variation greater than 20% of the mean set speed. Measurements were made over an analyser output frequency range of 0·05Hz to 40Hz.

RESULTS

The results of the measurements on the two motor speed-control systems are shown graphically in the form of Bode diagrams in Figs. 3 and 4. The diagrams show the relationship of both system loop gain and phase margin to frequency.

The principal features of the gain curve are the magnitude of the low-frequency gain, which determines the ability of the system to control speed to close limits when load changes take place relatively slowly, the frequency at which the gain begins to fall, and the frequency at which the gain reaches unity (zero on the dB scale in the figures).

The system phase margin is defined as the sum of the system open-loop phase shift and 180°. At the critical frequency when the phase shift is 180°, therefore, the phase margin will be zero. A system is stable provided the phase margin is positive when the gain is greater than zero dB. The Bode diagram shows the phase margin of the system at zero dB gain.

The Bode diagram in Fig. 3 shows that the tachometer system is stable at least for motor loads between one-third and full load at a speed of 500rev/min. The phase margins at zero dB gain are about 70° and 60° respectively. Examination of the motor curves (Ref. 1, Figs. 2a, 2b, and 2c) shows that the system loop gain has a maximum value in the operating region chosen for these tests. It is therefore reasonable to assume that as the system is stable in this region, it will be stable over the remainder of the operating range. Practical tests confirm this hypothesis.

The transfer curves for the armature-voltage system show that at full-load torque the phase margin is negative by about 20°. This operating condition corresponds with the condition of near-maximum loop gain, the worst state at which to test for stability. The system is not, in fact, unstable, for reasons which will be discussed later, but the circuit design could be improved to enable the system to function correctly with a positive phase margin.

The result of a minor change in the armature-voltage system is shown in the Bode diagram of Fig. 5. The phase margin is now about 60° at low load torque, rising to about 85° at full load. The circuit change is shown in the inset of Fig. 5, and entails the replacement of capacitor C_7 by the resistance-capacitance network shown. The way in which this network is incorporated into the armature-voltage system is shown in Fig. 8 (in the Appendix).

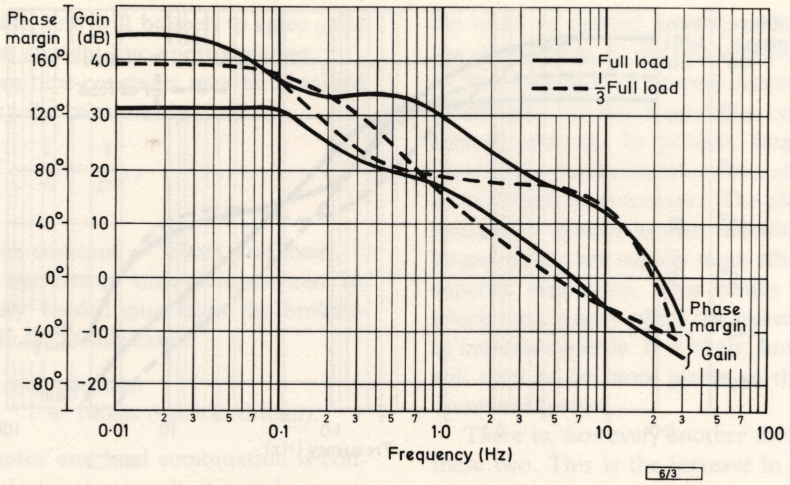

Fig. 3—Bode diagram for tachometer system

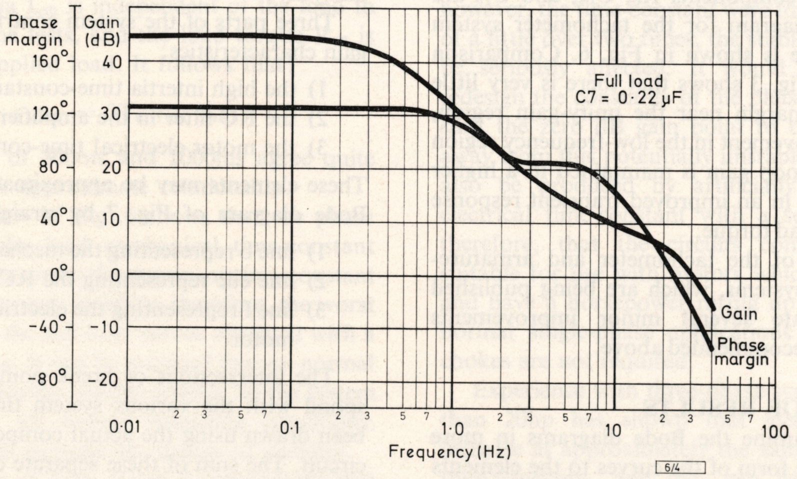

Fig. 4—Bode diagram for armature-voltage system

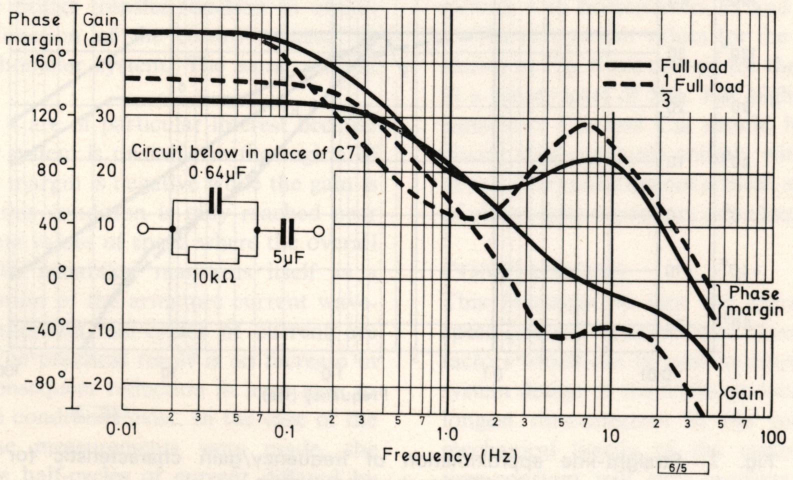

Fig. 5—Bode diagram for modified armature-voltage system

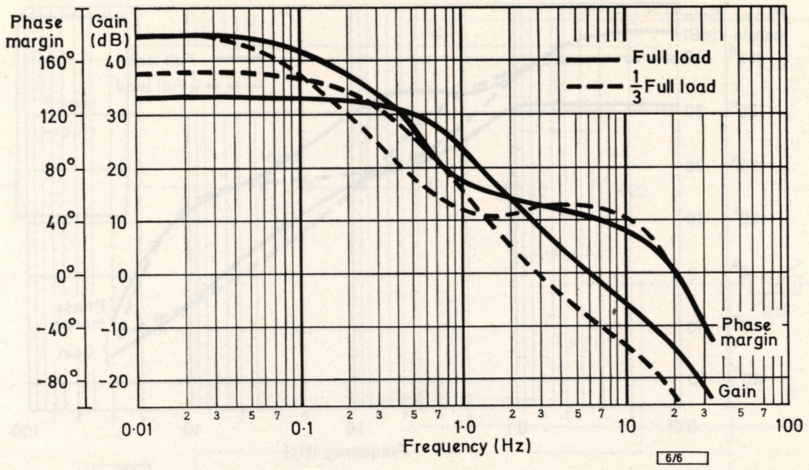

Fig. 6—Bode diagram for modified tachometer system

The network may also be used in the tachometer system, in which case components R_8, C_{14}, and C_{15} are removed. The Bode diagram for the tachometer system with the circuit change is shown in Fig. 6. Comparison of this diagram with Fig. 3 shows that there is very little change in the phase margin near the unity-gain region, but there is some improvement in the low-frequency region where the full system loop gain is maintained to a higher frequency. This results in an improved transient response to sudden changes in load torque.

Improved versions of the tachometer and armature-voltage speed-control systems, which are being published in Ref. 4, incorporate several minor improvements including the changes recommended above.

INTERPRETATION OF RESULTS

It is interesting to examine the Bode diagrams in more detail, and to relate the form of the curves to the elements of the speed-control system. The system represented by Fig. 6 is used as an example, since it lends itself to simple analysis.

Three parts of the system contribute to the frequency/gain characteristics:

1) the high intertia time-constant,
2) the RC filter in the amplifier feedback path,
3) the motor electrical time-constant.

These elements may be approximately represented on the Bode diagram of Fig. 7 by straight-line graphs, that is:

1) line b representing the mechanical time-constants,
2) line cde representing the RC filter,
3) line f representing the electrical time-constant of the motor.

The intersections or break points of these lines correspond with the various system time-constants and have been drawn using the actual component values of the test circuit. The sum of these separate characteristics gives the overall system curve aghikl as shown. The measured curve is shown as a broken line, and will be seen to agree quite well with the theoretical straight-line approximation.

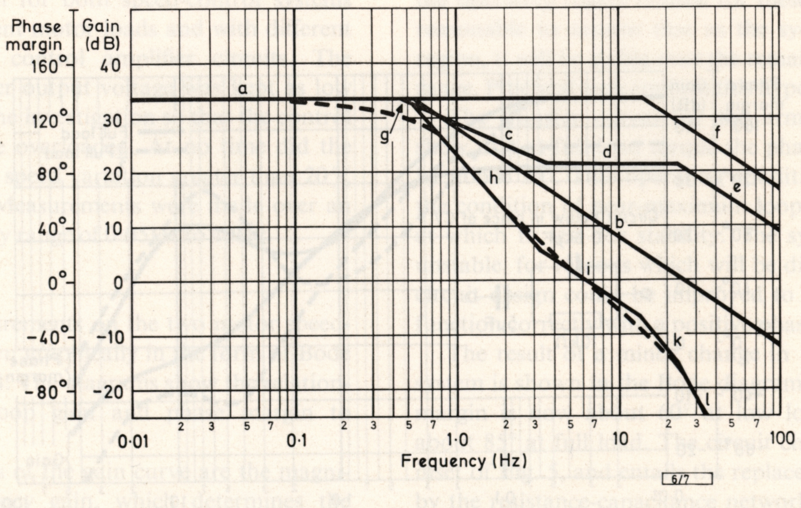

Fig. 7—Straight-line approximation of frequency/gain characteristic for modified tachometer system
Full lines: approximation; broken lines: measured characteristic

The individual system time-constants may be obtained from the graph by using the relationship:

$$T = \frac{1}{\omega} = \frac{1}{2\pi f},$$

from which:

motor mechanical time-constant = 300ms (full load).

In a similar way, the motor time-constant can be obtained for the lightly loaded case from the broken-line characteristic of Fig. 6. In this case:

motor mechanical time-constant
= 100ms (one-third load).

If the mechanical motor and load combination is considered in terms of an electrical network, it may be represented quite accurately by a lumped circuit of inductance and resistance where the mechanical time-constant:

$$T_m = L_m/R_m.$$

The effective intertia L_m is independent of the load in the system used for the tests, and the load torque R_m is proportional to the applied load. It follows that:

$$T_{m(\text{one-third load})} = 3T_{m(\text{full load})}.$$

The measured values of 300ms and 1000ms agree quite satisfactorily with this approximate relationship.

The transfer function of Fig. 6 shows that the phase margin increases as the load mechanical time-constant increases, so that this becomes the dominant time-constant in the sytem. For the system stability, therefore, the worst case is represented by the full-load curves obtained with a load of very low inertia. It can be assumed that no normal load will have a significantly smaller inertia, so the system will be stable under all normal operating conditions. Large-inertia loads will increase the degree of stability.

The Bode diagrams of Figs. 4 and 5, particularly that of Fig. 5, show that the phase characteristics of the armature-voltage bridge pass through a zero phase shift point at the balance point, and have phase lag and lead characteristics at lower and higher frequencies respectively. The transfer functions of other elements in the system must be added to the bridge transfer function to obtain the overall transfer function of the control system, as described for the tachometer system. The same general results are obtained.

The curves of Fig. 4 are of particular interest because they indicate that the system is unstable in the region of 25Hz where the phase margin is negative while the gain is positive. In practice, this condition is only reached near full load at intermediate values of speed where the overall loop gain is high. The instability manifests itself as a low-frequency modulation of the armature current waveform; in this case, alternate half-cycles of current are larger in amplitude. The practical result is an increase in motor losses and a consequent reduction in loop gain to the point where stable conditions exist. In the case of the drive on which these measurements were made, the amplitude of alternate half-cycles of current differed by only 20% at full load. The effect was largely masked by the onset of current limiting which progressively reduced the overall gain as the full-load point was reached.

Several points of general interest, relating to the effects of different motors on stability conditions, apply to both control systems. In general, larger horsepower motors have larger mechanical inertia and therefore higher values of minimum time-constant. The phase margin is increased, leading to greater system stability. On the other hand, larger motors are usually more efficient and therefore have superior regulation. This results in a higher loop gain which may largely offset the increase in phase margin due to increased inertia. It is likely, however, that large motors will tend to be more stable as the inertia is usually the dominant factor.

There is, however, another factor which may override these two. This is the increase in armature time-constant which often accompanies an increase in motor horsepower. In the Bode diagram of Fig. 7, it will be seen that the influence of motor electrical time-constant is represented by line f. In this case it only affects the transfer function in the region to the right of the zero dB gain point. If, however, the time-constant were to be increased by a factor of a little over two times, the stability of the system would be seriously affected. It would then be necessary to redesign the constants of the phase correction network to shift the zero dB gain point to the left of the diagram, away from this potentially unstable region. This effect will also be produced by artificially increasing the motor electrical time-constant with a series choke. It follows, therefore, that the circuits considered here are only suitable for use with motors which have no series choke and have a horsepower rating up to 20hp, that is for all normal single-phase applications where series armature chokes are not required.

Experience with three-phase systems and motors larger than 20hp has shown that mechanical time-constants increase at approximately the same rate as the electrical time-constants, and they can be related to the motor horsepower by the relationship:

$$T_2 = T_1\left[\frac{P_2}{P_1}\right]^{\frac{1}{2}},$$

where T_1 and T_2 are the mechanical time-constants of motors with horsepowers P_1 and P_2 respectively.

The component values for the improved filter network shown in Fig. 8 are correct for the typical motor and load at a power level of 5hp. For higher powers, the values of capacitors C_{19} and C_{20} should be increased so that the circuit time-constants comply with the relationship given above. The values are not critical, and the normal tolerances of electrolytic capacitors are adequate.

CONCLUSIONS

This investigation into the dynamic stability of motor speed-control systems has revealed several important factors which can be used as empirical rules of thumb for system design. If the feedback loop is designed so that the longest time-constant in the loop is provided by the mechanical inertia of the motor, any increase in this time-constant will only improve the overall stability of the system. The stability of the feedback control loop is affected by both the mechanical load and the electrical time-constant of the motor armature winding, and so the system design must take both into account. Provided that systems with a very high gain are not involved, and that motors of normal design are being used, then it is possible to design feedback loops suitable for a wide range of motor powers which will be stable with all frictional and inertial loads without a detailed knowledge of the load or motor.

REFERENCES

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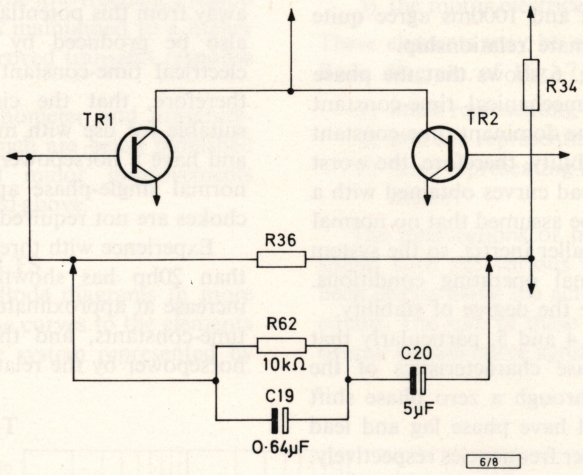

Fig. 8—Incorporation of modified filter network into practical system. The component references are those on the system circuit diagram

APPENDIX
DETAILS OF MODIFIED FILTER NETWORK

Details of the circuit modifications to incorporate the improved filter network in the tachometer and armature-voltage systems are given below.

Tachometer system

Remove components R_8, C_{14}, and C_{15}. Resistors R_9 and R_{27} can now be combined into one component with a value of 3·3kΩ. The filter network R_{62}, C_{19}, and C_{20} is connected across R_{36}, as shown in Fig. 8.

Armature-voltage system

Remove capacitor C_7. The network R_{62}, C_{19}, C_{20} is connected in place of capacitor C_7, as shown in Fig. 8.

Component types

The components used in the modified filter network are:

R_{62}	10kΩ, ¼W
C_{19}	0·64μF, Mullard type C426AS/H0·64
C_{20}	5·0μF, Mullard type C426AR/H5

The components can be accommodated on the printed-wiring board No. 14242–2 in place of capacitor C_7, with the positive ends of the electrolytic capacitors towards the terminal strip or edge connector.